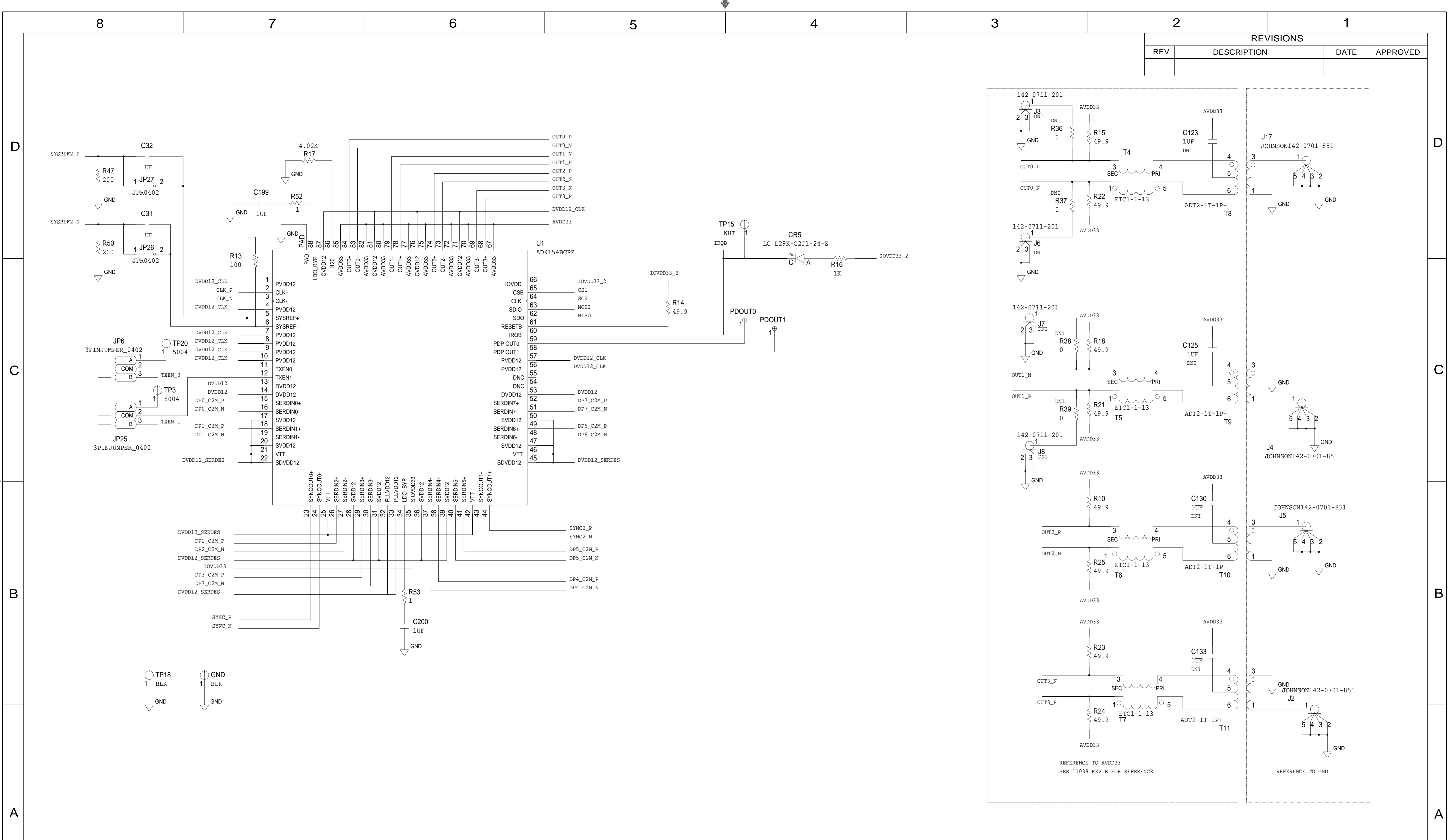


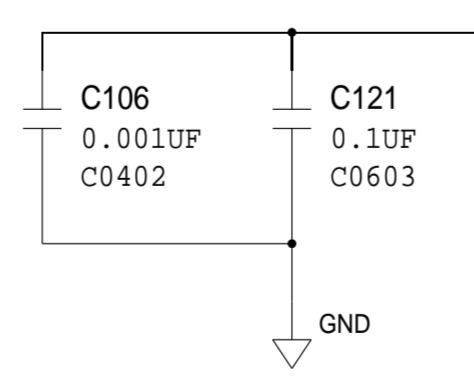
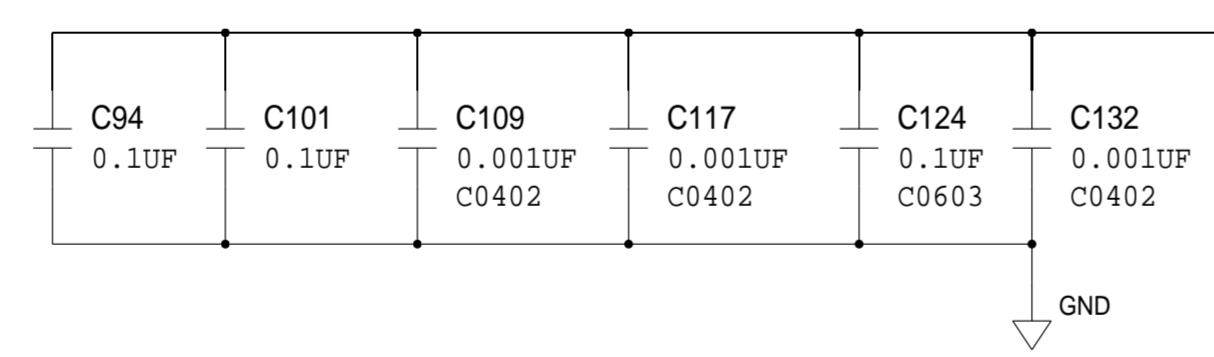
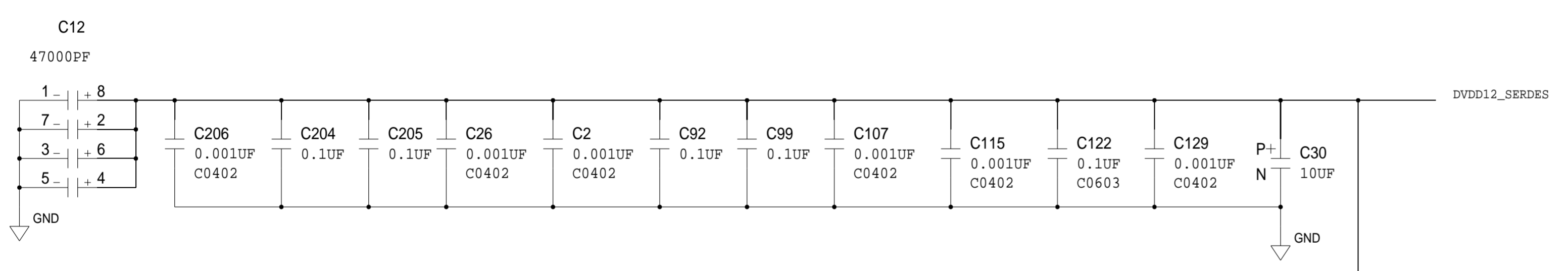
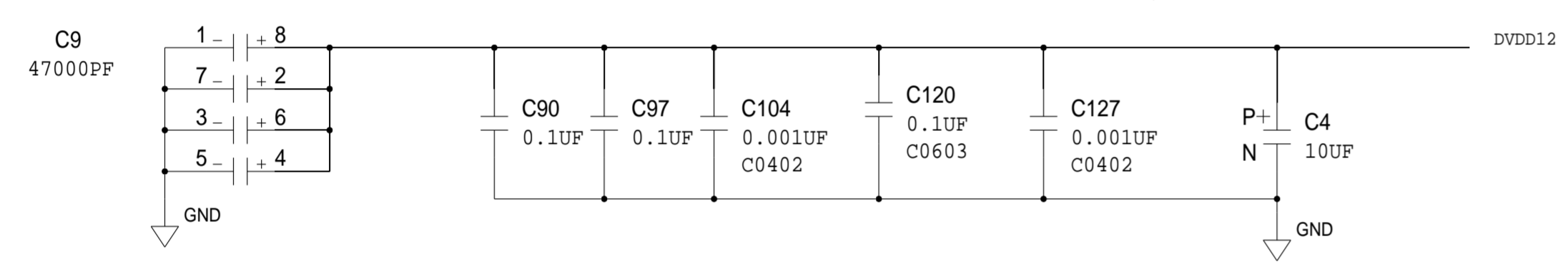
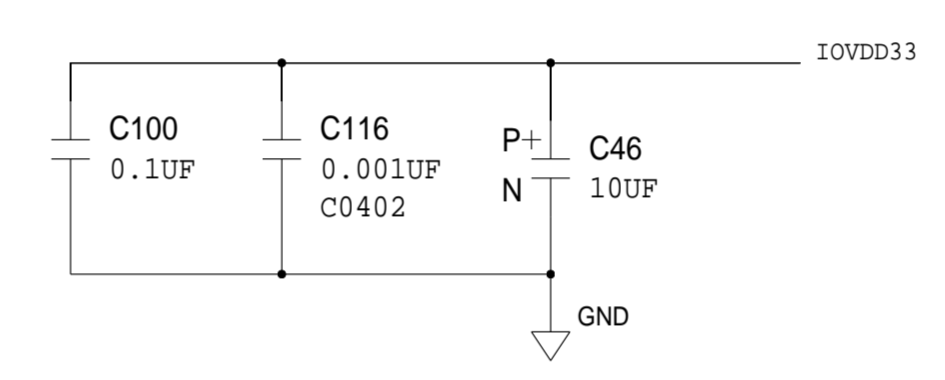
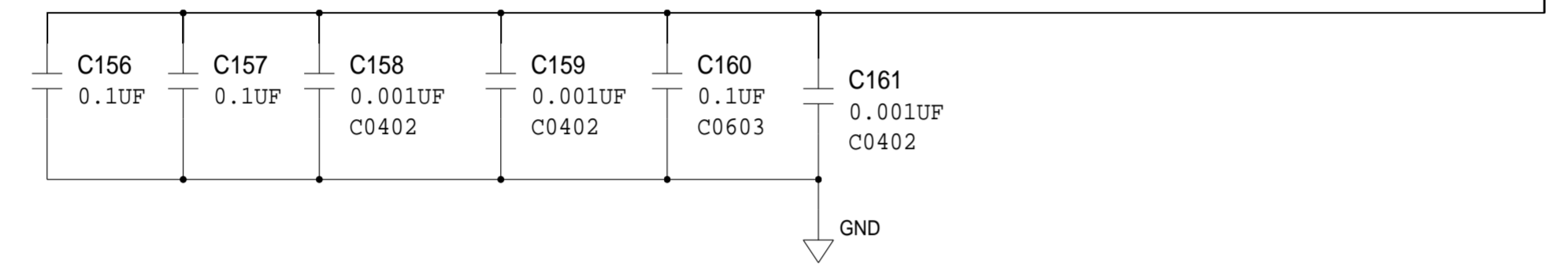
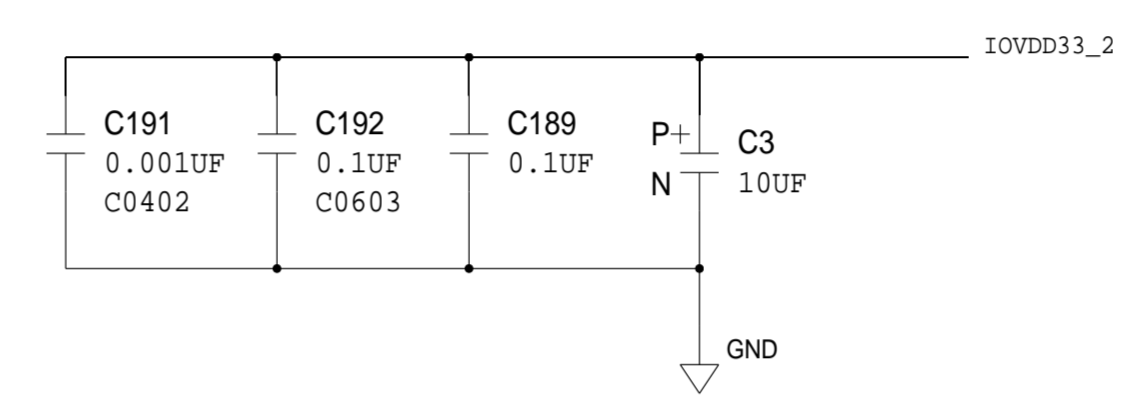
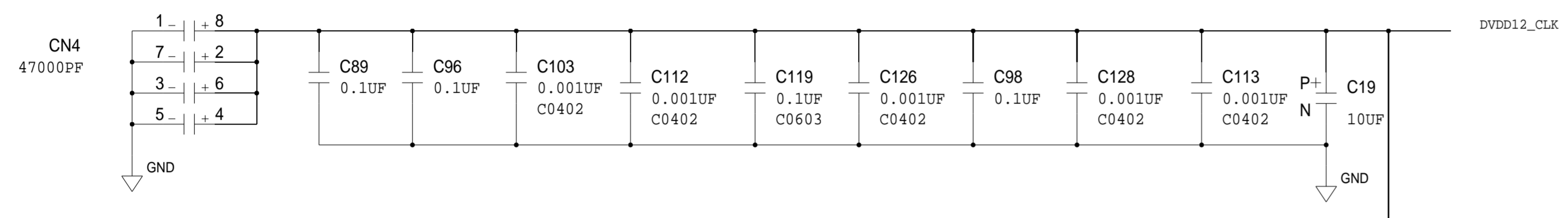
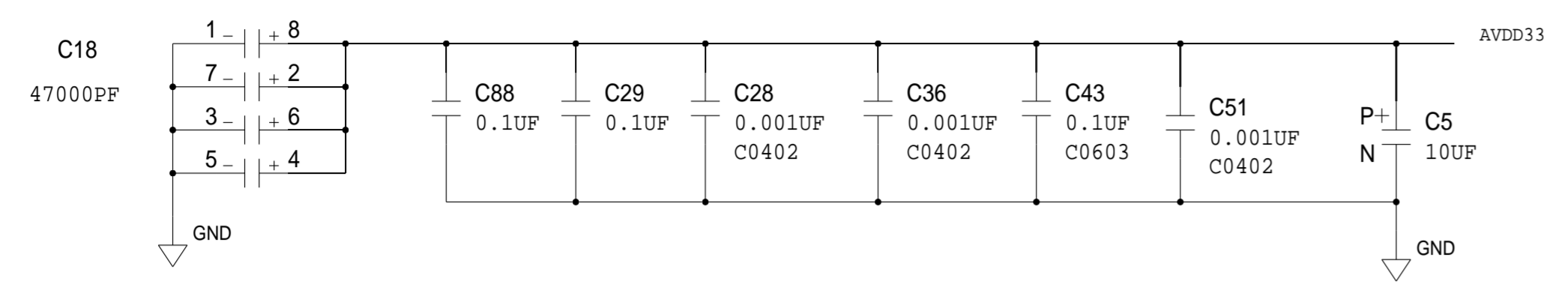


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 14024	REV A	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 2 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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PTD ENGINEER <PTD_ENGINEER>	SIZE <b>D</b>	SCALE <SCALE>	
		SHEET 3 OF 8	

FMC

P1 ASP-134488-01

P1 ASP-134488-01

P1 ASP-134488-01

P1 ASP-134488-01

P1 ASP-134488-01

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

D

C

D

C

"A" ROW CLOSEST TO BOARD EDGE

ON 3P3V, 12P0V, AND VADJ, HAVE PIN-HEADER JUMPER BETWEEN FMC PINS AND REST OF BOARD, TO ALLOW FOR CURRENT MEASUREMENT PER RAIL.

P1 ASP-134488-01

P1 ASP-134488-01

P1 ASP-134488-01

P1 ASP-134488-01

P1 ASP-134488-01

B

A

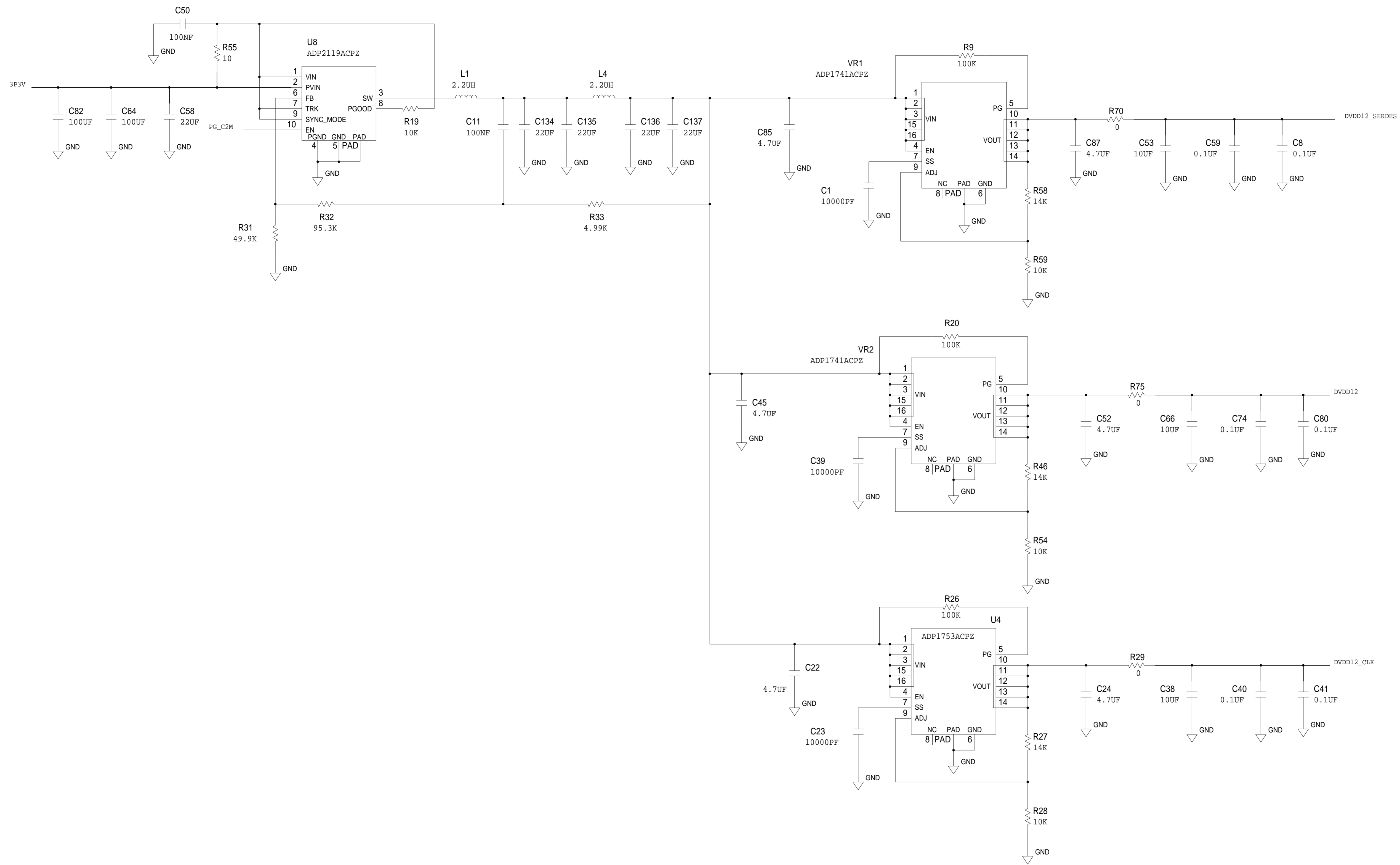
B

A

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PTD ENGINEER <PTD_ENGINEER>	SCALE <SCALE>	SHEET 4 OF 8	

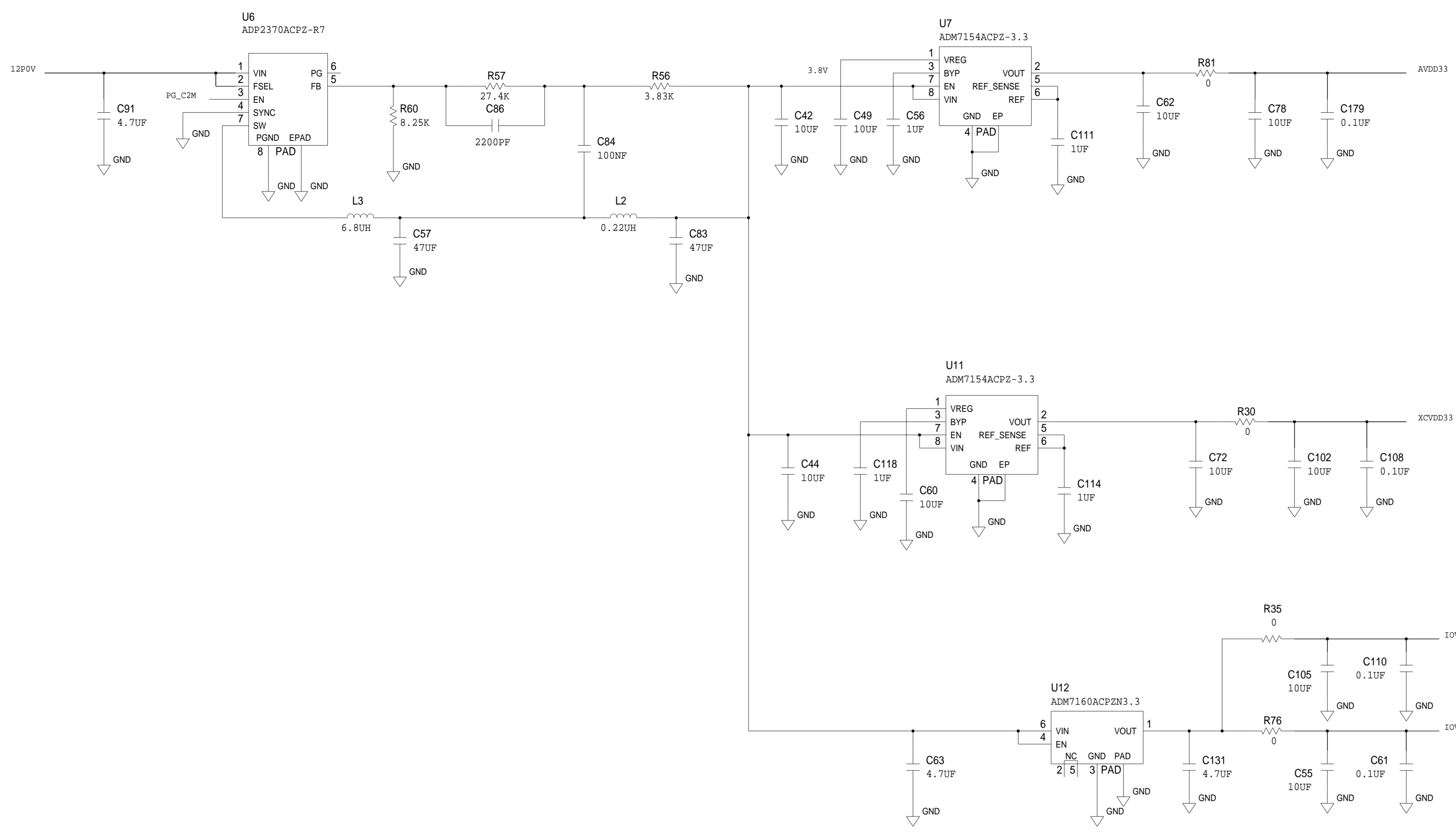
VIO\_B\_M2C PINS SHOULD HAVE WIDE ETCH CONNECTION TO VADJ PINS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

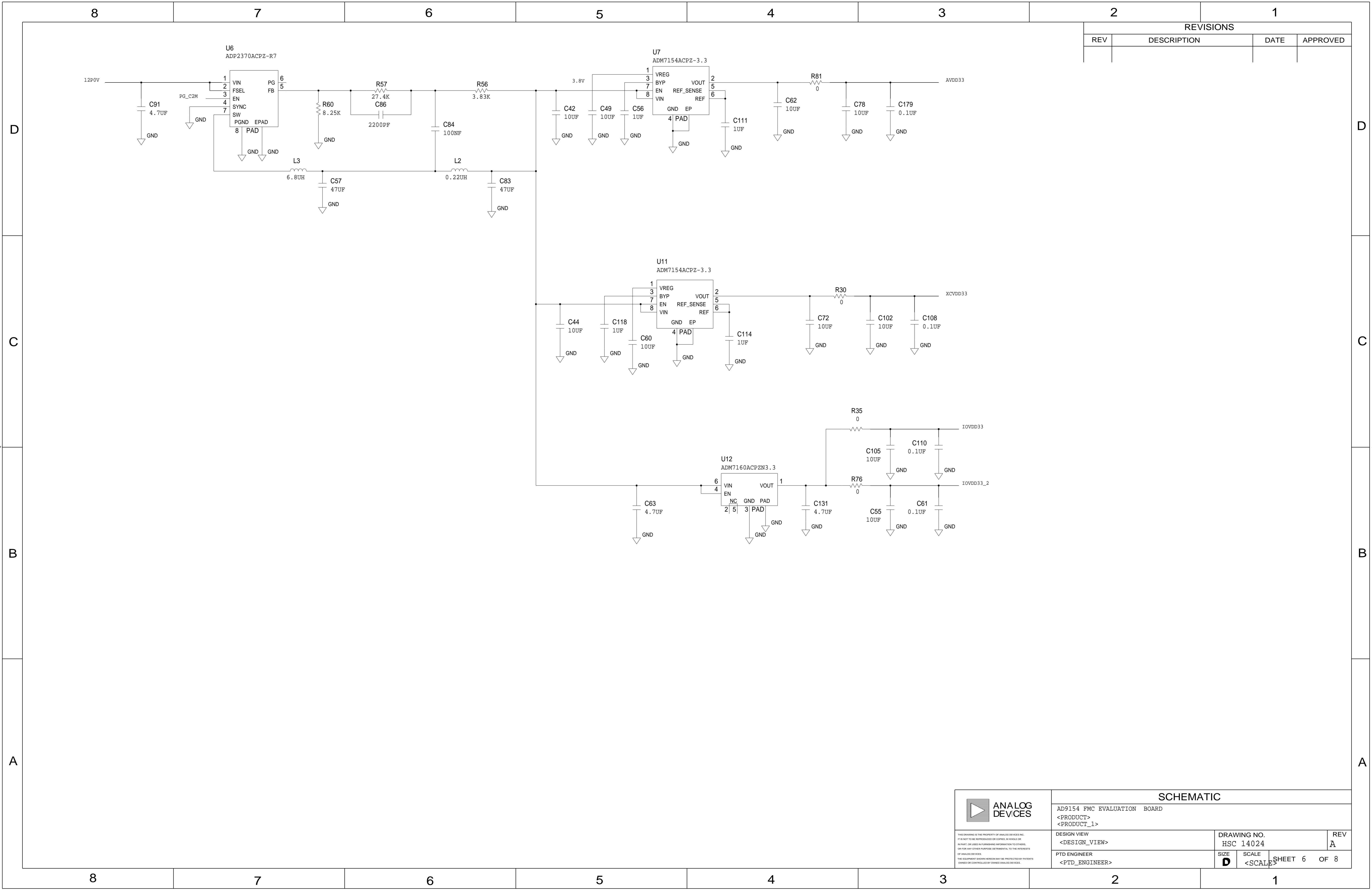


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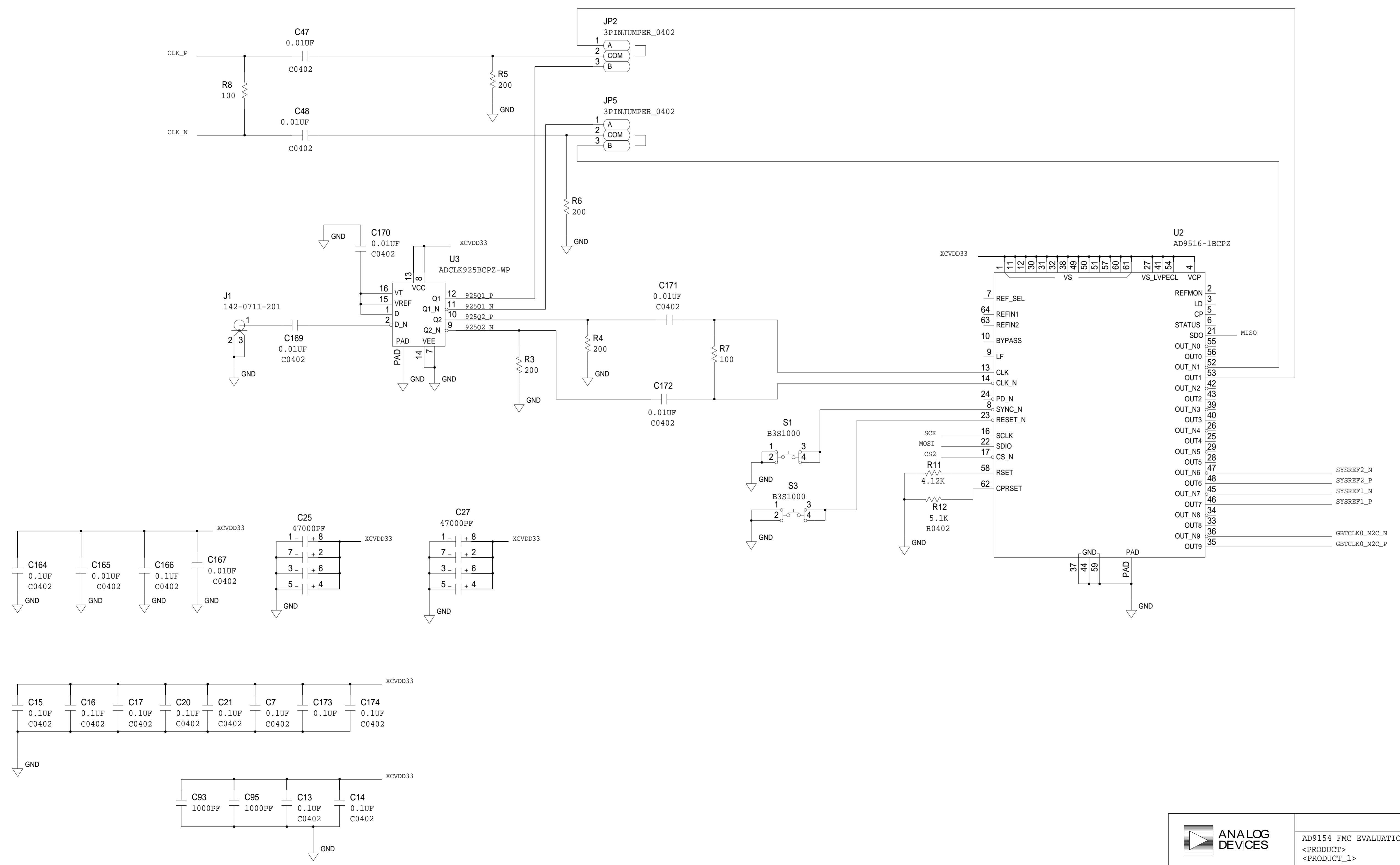
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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SHEET 6 OF 8			



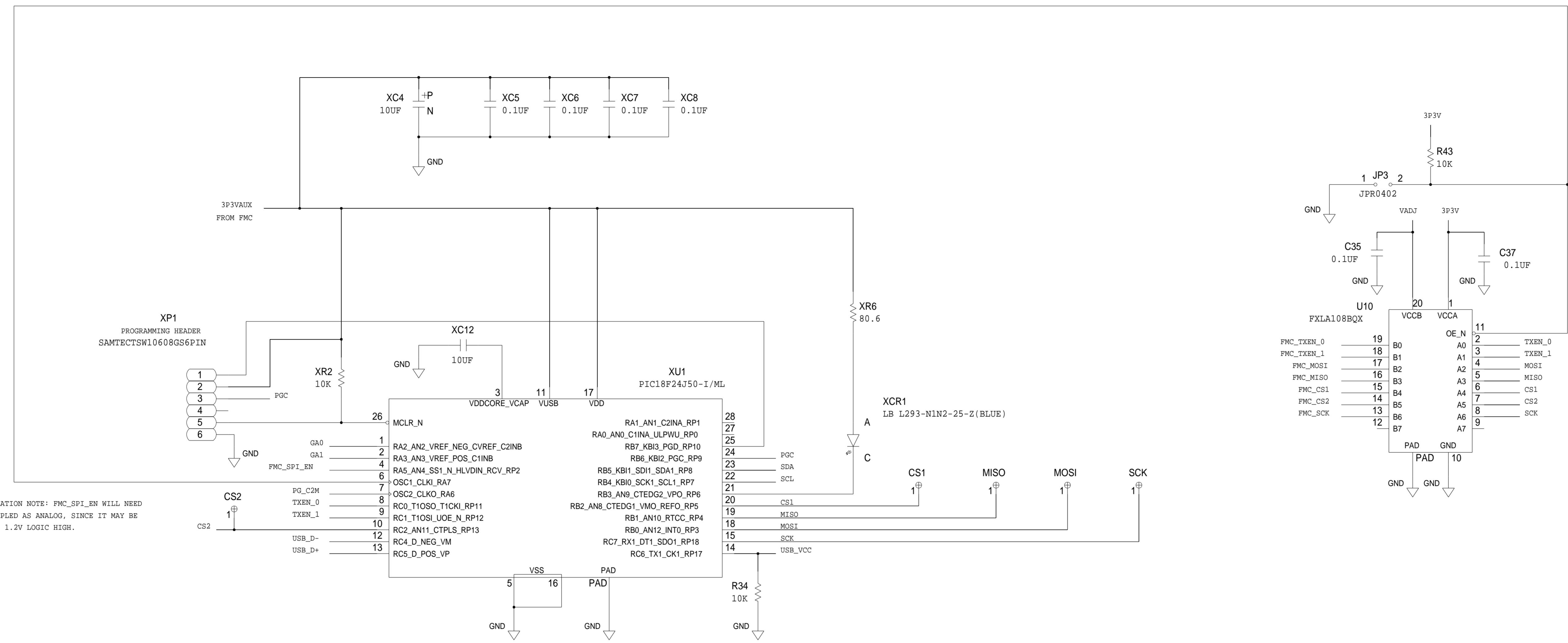
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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		SHEET 7 OF 8	

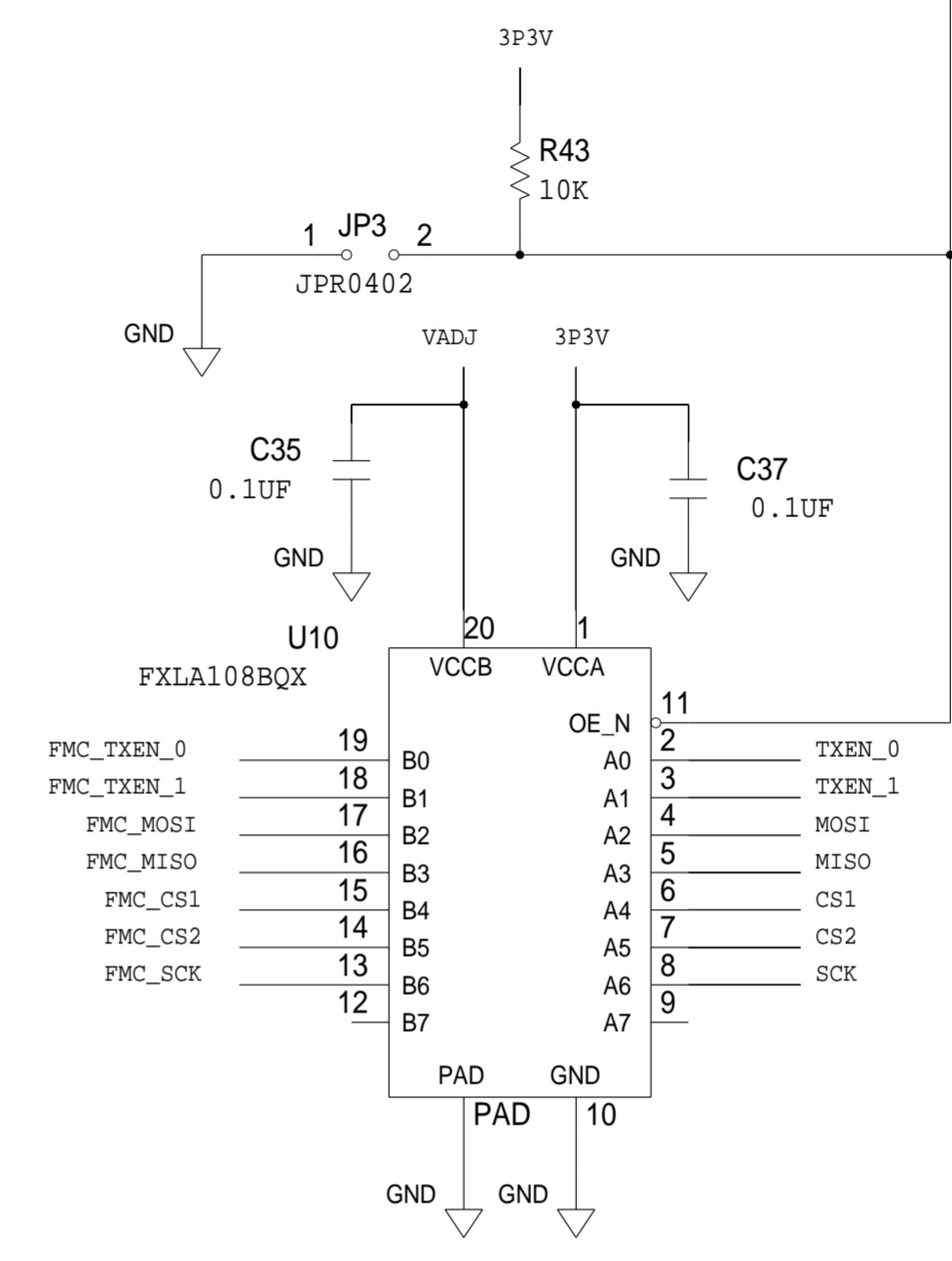
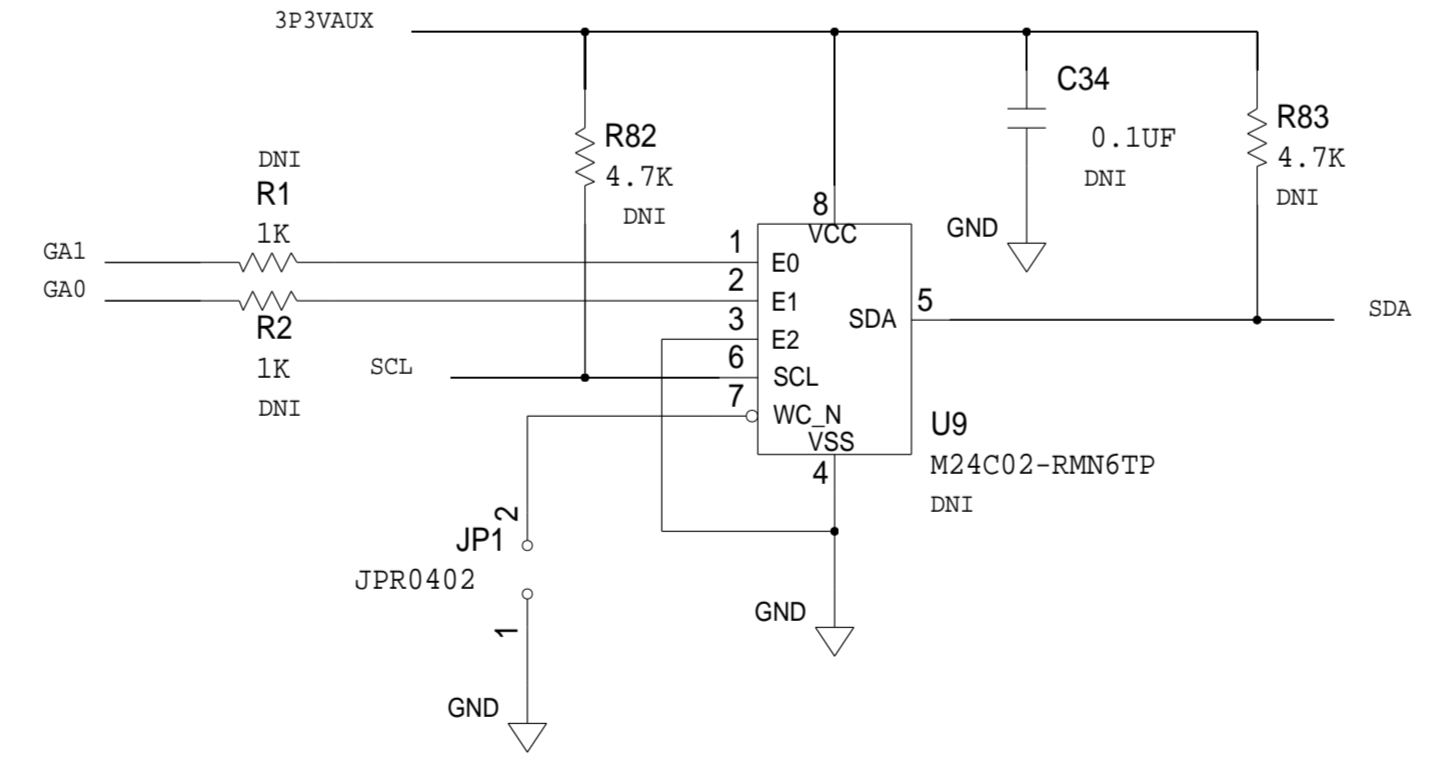
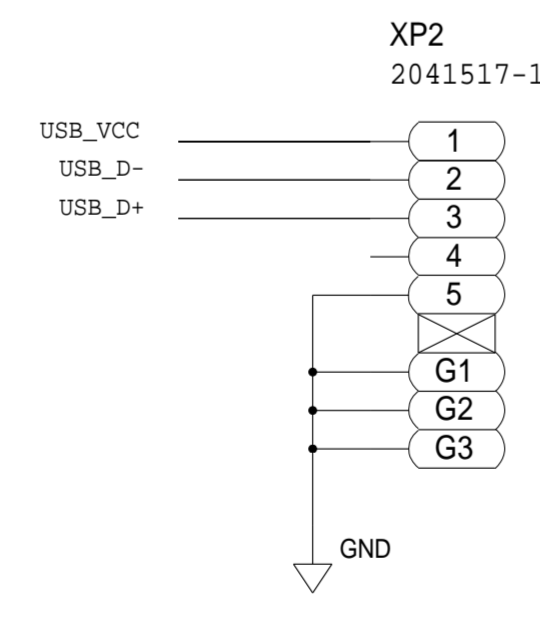
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IMPLEMENTATION NOTE: FMC\_SPI\_EN WILL NEED TO BE SAMPLED AS ANALOG, SINCE IT MAY BE AS LOW AS 1.2V LOGIC HIGH.

NOTE:  
 IF USB CABLE IS PLUGGED IN PIC IS THE SOURCE OF SPI BUS AND TXEN SIGNALS  
 IF USB IS UNPLUGGED FMC INTERFACE IS THE SOURCE OF SPI BUS AND TXEN SIGNAL.



	<b>SCHEMATIC</b>		
	AD9154 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 14024	REV A
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 8 OF 8