RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	16AUG24	D.SUDOY
B	CHANGES AS PER ECR-123869	03APR25	D.SUDOY
B1	CHANGES AS PER ECR-125997	31JUL25	D.SUDOY

AD-ETHERNETPLDEVICE-SL
PCB-1
POWER AND 10BASE-T1L

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

	DATE
TEMPLATE ENGINEER -	
HARDWARE SERVICES M. VALE	16AUG24
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER K. EMPENSANDO	16AUG24
TEST PROCESS -	
HARDWARE RELEASE K. JABATAN	16AUG24
DESIGNER D. VILLANUEVA	16AUG24
PTD ENGINEER D. SUDOY	16AUG24
CHECKER -	

SCHEMATIC

ANALOG DEVICES

HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110
PACKAGE : LeadCount-lead BodySize PackageType-family
: Pitch-pitch StyleVendor Style
<User Define>
<User Define>
<User Define>

MASTER PROJECT TEMPLATE: TBD
TESTER TEMPLATE: 067706_a

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS: X.XX +-0.010, X.XXX +-0.005
FRACTIONS: +-1/32
ANGLES: +-2

DRAWING NO. 02_083152
REV. B

SIZE D | SCALE 1:1 | CODE ID NO. CodeID | SHEET 1 OF 8

AD-ETHERNETAPLDEVICE-SL - BLOCK DIAGRAM

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ETHERNET CONNECTOR
SHIELD
DIN-B CHASSIS EARTH
CM
POLARITY PROTECTION
DM
<2:2>
<2:2>
POWER LINE
LOAD_P
SHUNT
LOAD_N
LT8440
POWER LIMITER
COUPLING CAPACITORS
I2C
OPTIONAL
For Development/ Debugging Only
To MAX32690
SWD
To MAX32690
ADIN1110
TX/RX
1.8V
SRAM
1.8V
FLASH
HYPERBUS
QSPI
SPI 3
MCU_TEMP
MAX6613
TEMPERATURE SENSOR
SUP_3.3V
LOAD_E
ADP123
LDO
3.5V
MAX32690
PROCESSOR
3.3V
1.8V
1.1V
EXTERNAL SPI CONNECTOR
SPI 1
SPI 1
SPI 0
≥1.8k
I2C/WATCHDOG
RESET_OUT
SUPERVISOR
MAX42500
MONITOR
SUP_3.3V
3.3V
1.8V
1.1V
SPI_2_security
LOAD_E
ADuM1441
ISOLATION
3.3V
3.3V_iso
iso
ISOLATED DOMAIN
MAX01065
SECURITY CHIP
3.3V
TEMPERATURE SENSE CONNECTOR
SPI 0 iso
ADFS7124-4
ADC
ADP151
3.3V iso
LDO
iso
≥3k
NTC
iso
x2
iso
MAX253
ISO-POWER
3.5V
LOAD_E
3.5V
x2
LOAD_N
LT8606
BUCK
LOAD_P
LOAD_N
3.3V
ADP151
LDO
3.5V
LOAD_N
1.8V
MAX17626
BUCK
3.5V
LOAD_N
1.1V
ADP151
LDO
3.3V
LOAD_N
SUP_3.3V
ADP151
LDO
3.5V
LOAD_E

Yellow area indicate the parts on the 2nd Board

Blue area indicate the circuit that must be intrinsically safe.

ANALOG DEVICES

SCHEMATIC

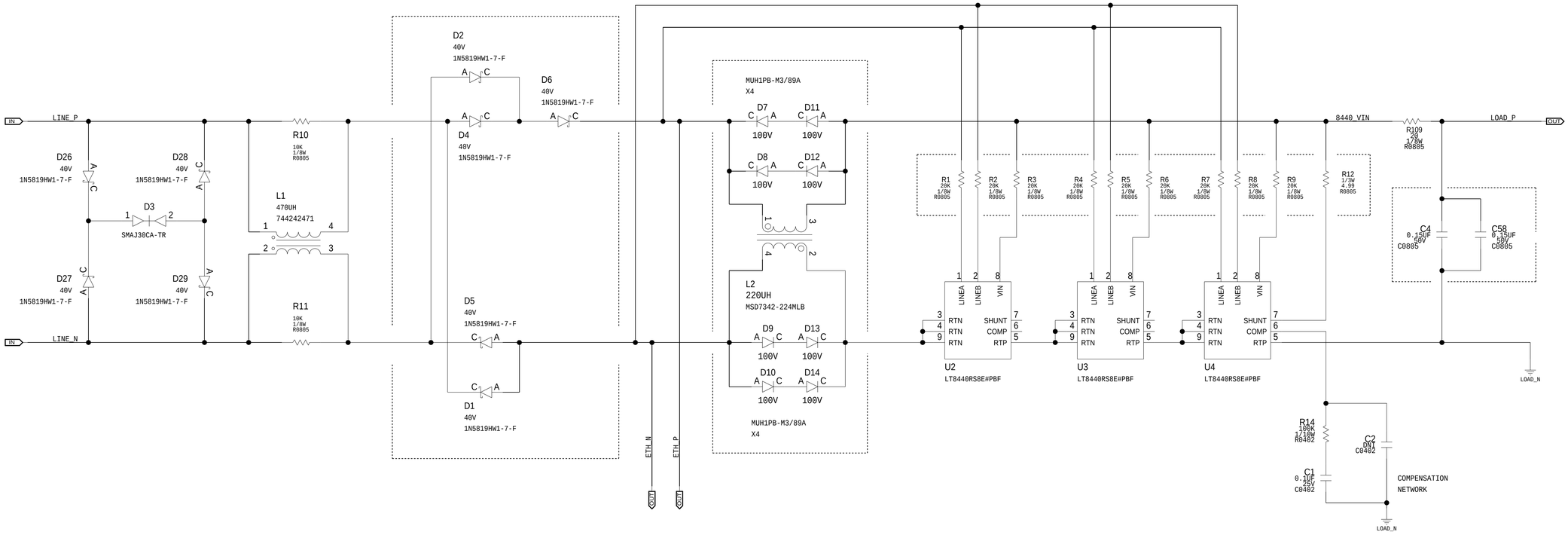
HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_083152	B

PTD ENGINEER	SIZE	SCALE	SHEET	OF
D. SUDOY	D	1:1	2	8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

INPUT AND POWER CONDITIONING PATH



LOAD_N = GROUND IN 1ST BOARD
LOAD_E = GROUND IN 2ND BOARD
ISO_GND = GROUND FOR ISOLATED CKT

LEGEND:

-------- OR 0.7MM MINIMUM CLEARANCE

INTRINSIC SAFETY CONSIDERED

ANALOG DEVICES

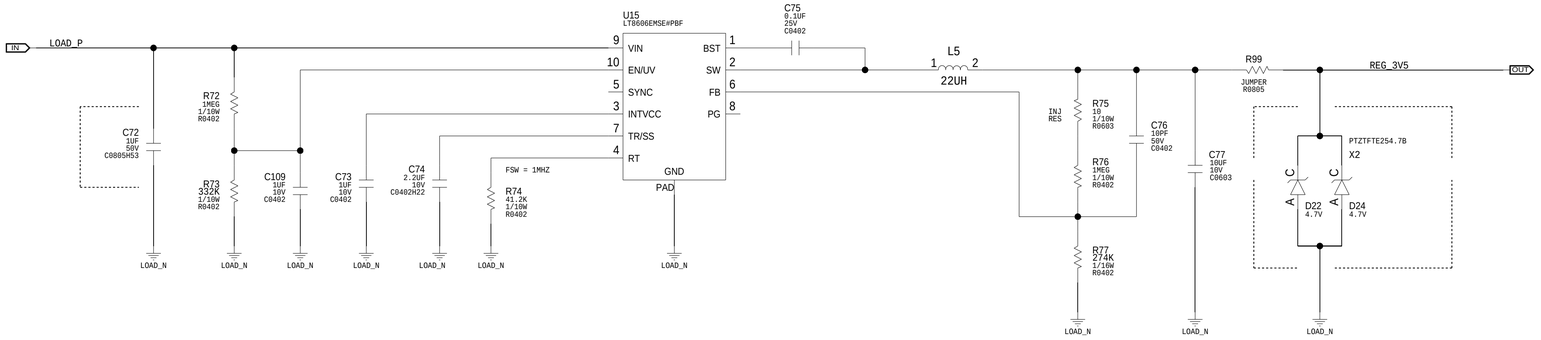
SCHEMATIC

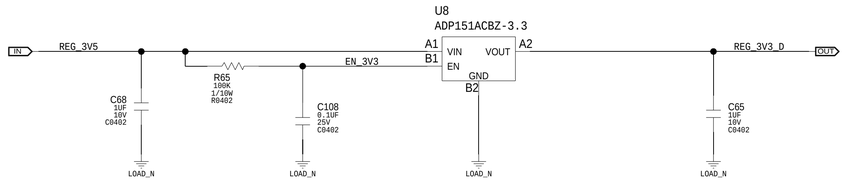
HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110

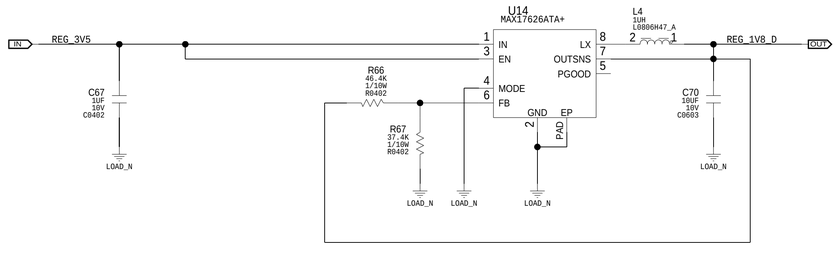
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_083152	B
PTD ENGINEER	SIZE / SCALE	SHEET 3 OF 8
D. SUDOY	D / 1:1	

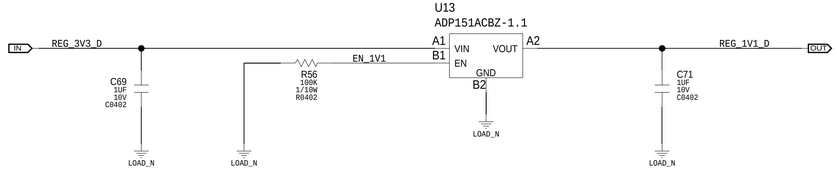
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER RAILS PATH
3V3, 1V8, 1V1









LOAD_N = GROUND IN 1ST BOARD
LOAD_E = GROUND IN 2ND BOARD
ISO_GND = GROUND FOR ISOLATED CKT

LEGEND:
-------- 0.7MM MINIMUM CLEARANCE
OR INTRINSIC SAFETY CONSIDERED

ANALOG DEVICES

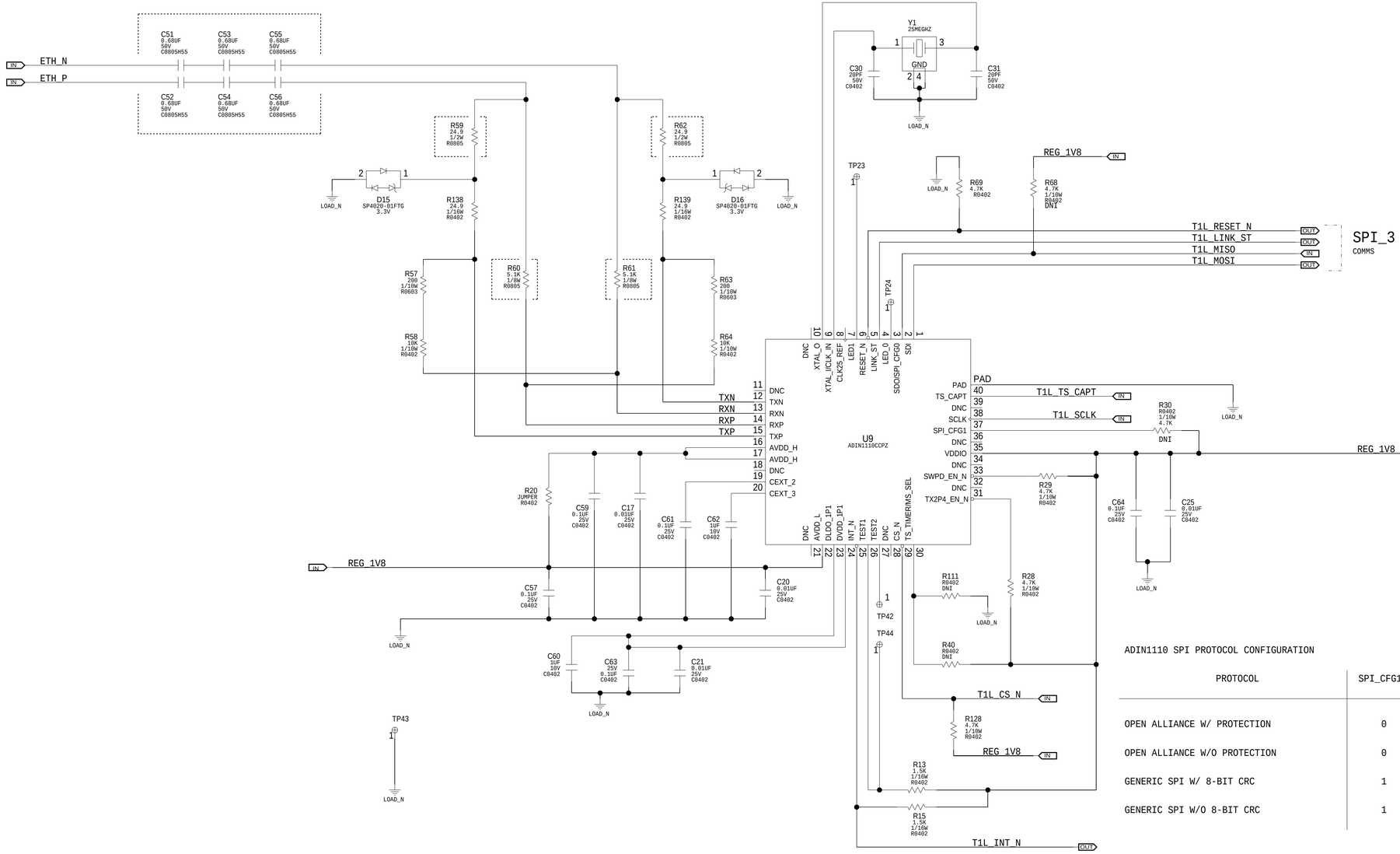
SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_083152	B
PTD ENGINEER: D. SUDOY	SIZE: D / SCALE: 1:1	SHEET 4 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

NETWORK SIGNAL PATH



ADIN1110 SPI PROTOCOL CONFIGURATION

PROTOCOL	SPI_CFG1	SPI_CFG0	R30	R68
OPEN ALLIANCE W/ PROTECTION	0	0	UNSTUFFED	UNSTUFFED
OPEN ALLIANCE W/O PROTECTION	0	1	UNSTUFFED	4.7K OHMS
GENERIC SPI W/ 8-BIT CRC	1	0	4.7K OHMS	UNSTUFFED
GENERIC SPI W/O 8-BIT CRC	1	1	4.7K OHMS	4.7K OHMS

LOAD_N = GROUND IN 1ST BOARD
LOAD_E = GROUND IN 2ND BOARD
ISO_GND = GROUND FOR ISOLATED CKT

LEGEND:
-------- OR 0.7MM MINIMUM CLEARANCE
INTRINSIC SAFETY SPECS CONSIDERED

ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_083152	B
PTD ENGINEER: D. SUDOY	SIZE D / SCALE 1:1	SHEET 5 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

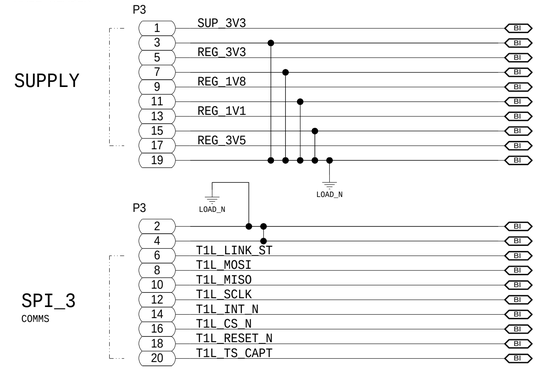
CONNECTORS

APL CONNECTOR
TERMINAL BLOCK

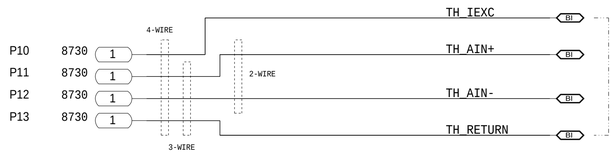
APL INPUT

FOR DIN-B FORM FACTOR
SHIELD GND IS CONNECTED EXTERNALLY

FW-10-03-G-D-200-200
MALE HEADER

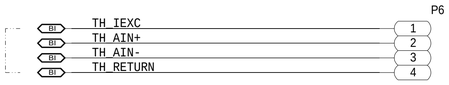


RTD OR THERMOCOUPLE SENSOR
TERMINAL BLOCK



PT100
SENSOR TO ADC

FW-02-03-G-D-200-200
MALE HEADER



LOAD_N = GROUND IN 1ST BOARD
LOAD_E = GROUND IN 2ND BOARD
ISO_GND = GROUND FOR ISOLATED CKT

SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110

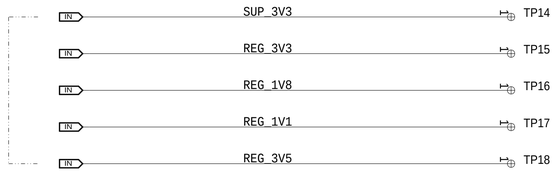
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_083152	B

PTD ENGINEER	SIZE	SCALE	SHEET
D. SUDOY	D	1:1	SHEET 6 OF 8

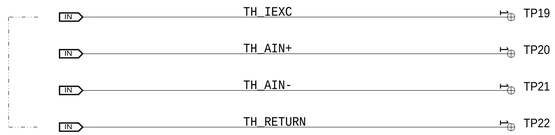
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

TEST POINTS

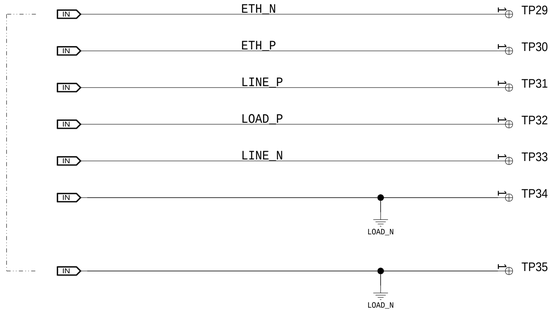
POWER



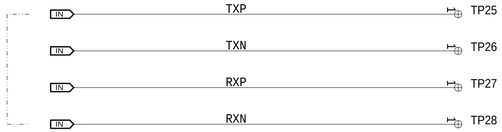
TEMPERATURE SENSOR



APL LT8440



ADIN1110



SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_083152	B

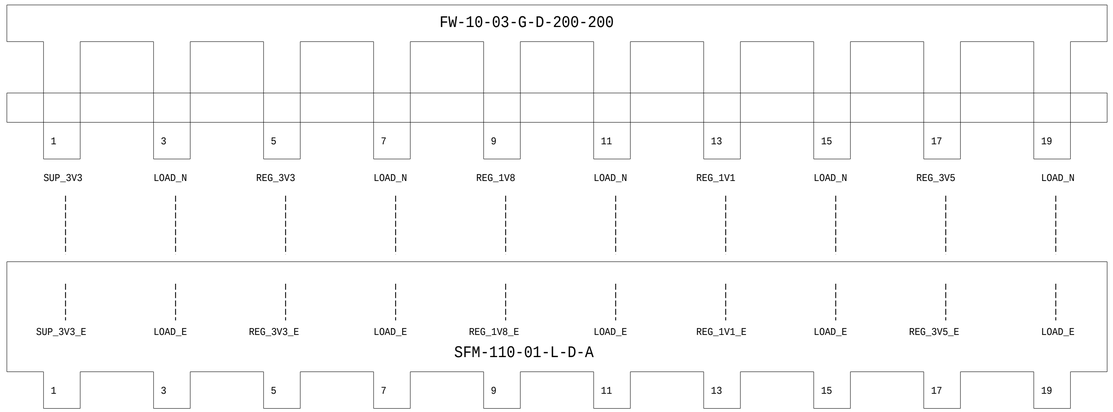
PTD ENGINEER	SIZE	SCALE	SHEET
D. SUDOY	D	1:1	SHEET 7 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

INTERCONNECTION OF TWO BOARDS

P3

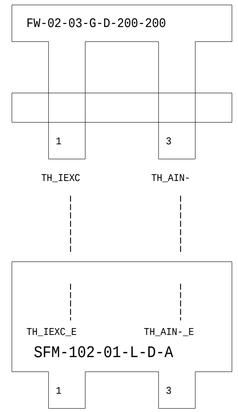
PCB-1
ODD PINS



PCB-2
ODD PINS

P5

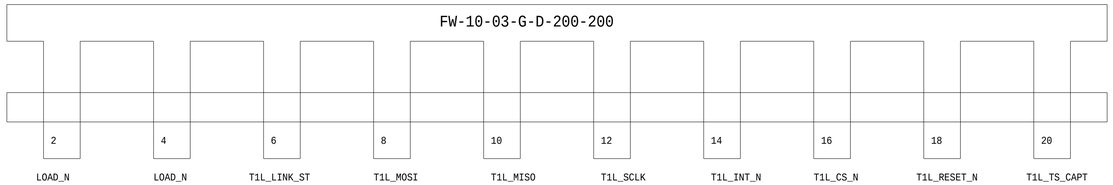
P6



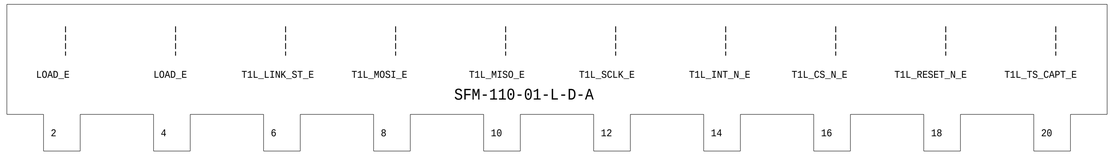
P7

P3

PCB-1
EVEN PINS

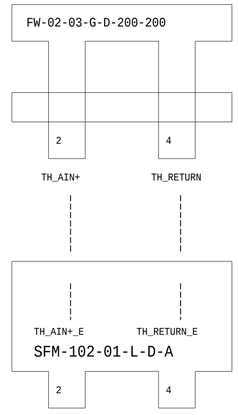


PCB-2
EVEN PINS



P5

P6



P7

ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): LT8440
: ADIN1110

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_083152	B

PTD ENGINEER	SIZE	SCALE	SHEET
D. SUDOY	D	1:1	SHEET 8 OF 8