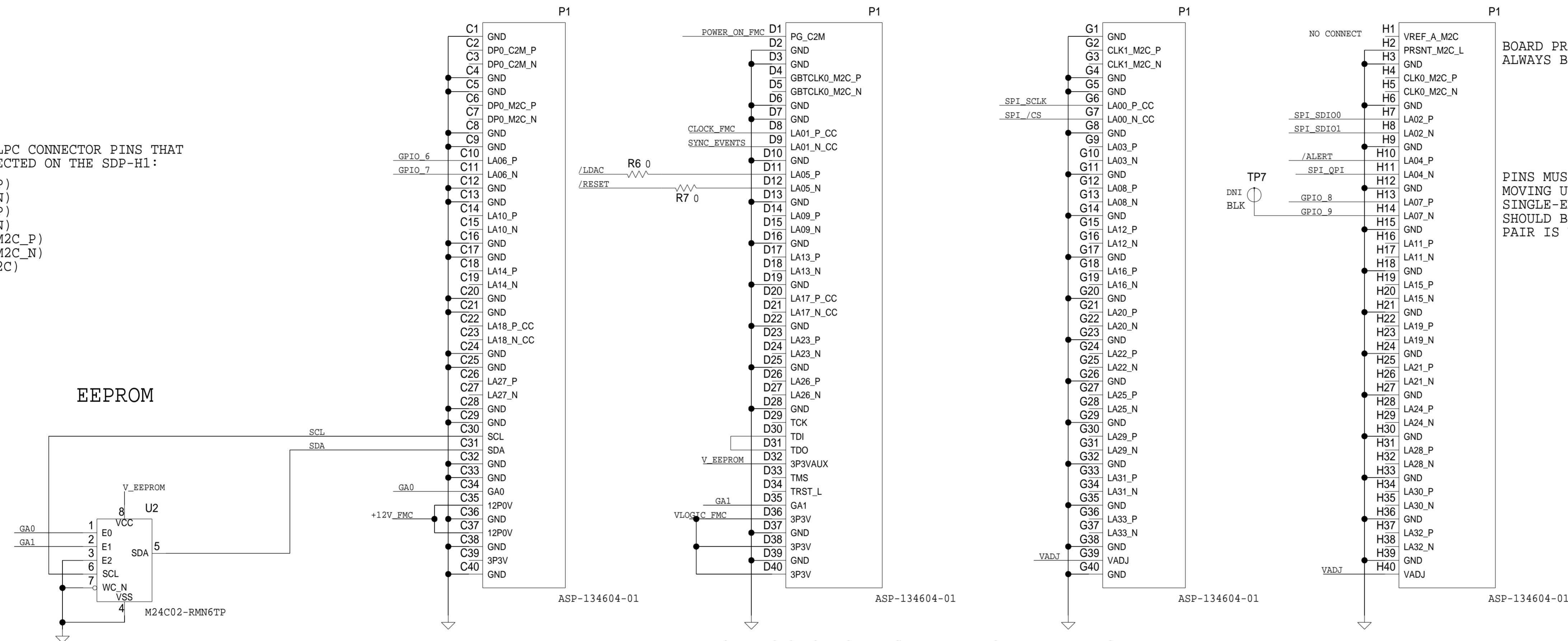


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FPGA FMC CONNECTIONS

LIST OF FMC-LPC CONNECTOR PINS THAT ARE NOT CONNECTED ON THE SDP-H1:

- C2 (DP0_C2M_P)
- C3 (DP0_C2M_N)
- C6 (DP0_M2C_P)
- C7 (DP0_M2C_N)
- D4 (GBTCLK0_M2C_P)
- D5 (GBTCLK0_M2C_N)
- H1 (VREF_A_M2C)



BOARD PRESENT PIN (H2) MUST ALWAYS BE TIED TO GROUND

PINS MUST BE ASSIGNED STARTING WITH LA00 AND MOVING UP THE LA BUS UNTIL IT IS FULL. WHEN SINGLE-ENDED SIGNALING IS USED, THE _P LINE SHOULD BE USED BEFORE THE _N LINE OF THE SAME PAIR IS USED.

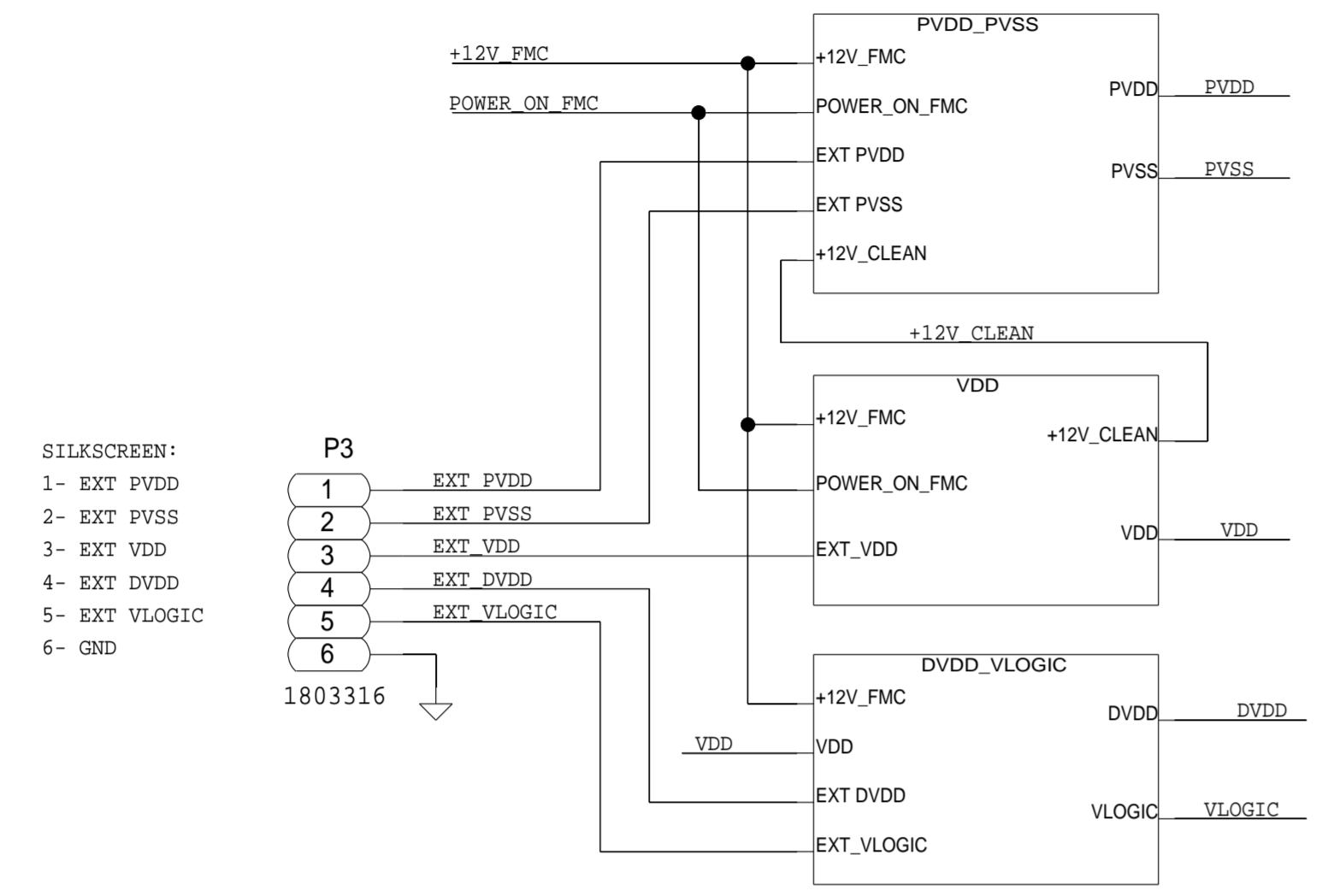
IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN

POWER SUPPLIES:
 12P0V. 1A MAX CURRENT LIMIT
 3P3V. 3A MAX CURRENT LIMIT
 VADJ. 2A MAX CURRENT LIMIT. 1.2V TO 3.3V.

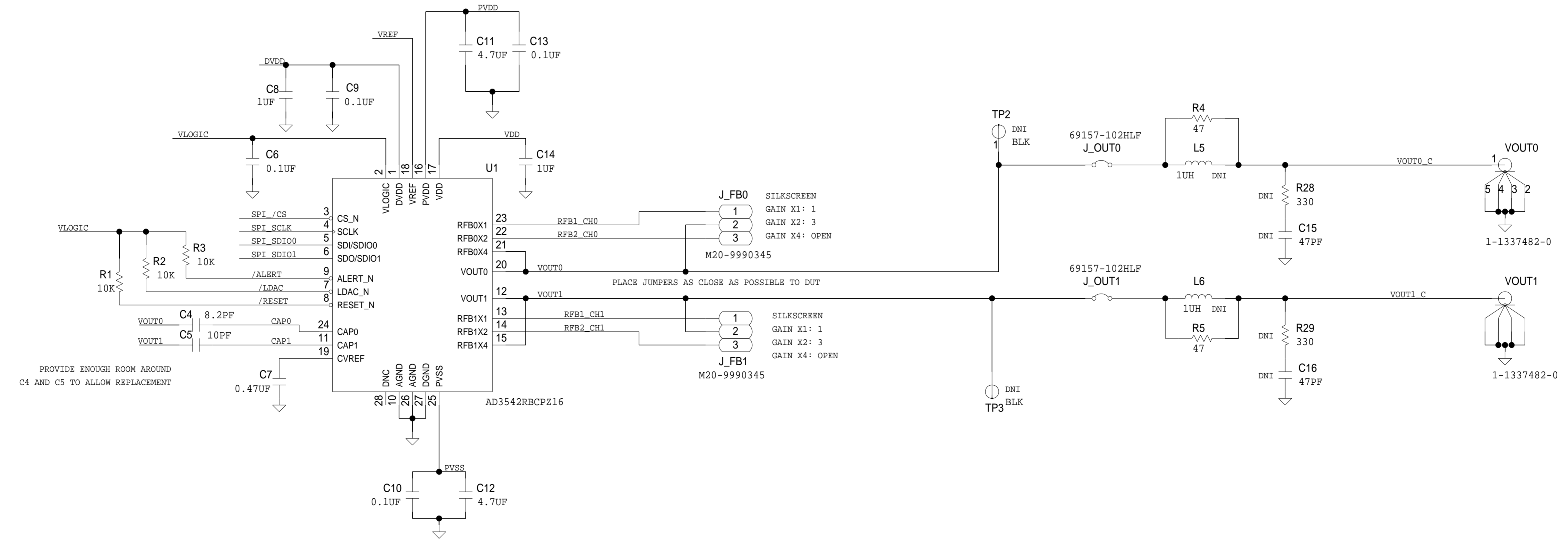
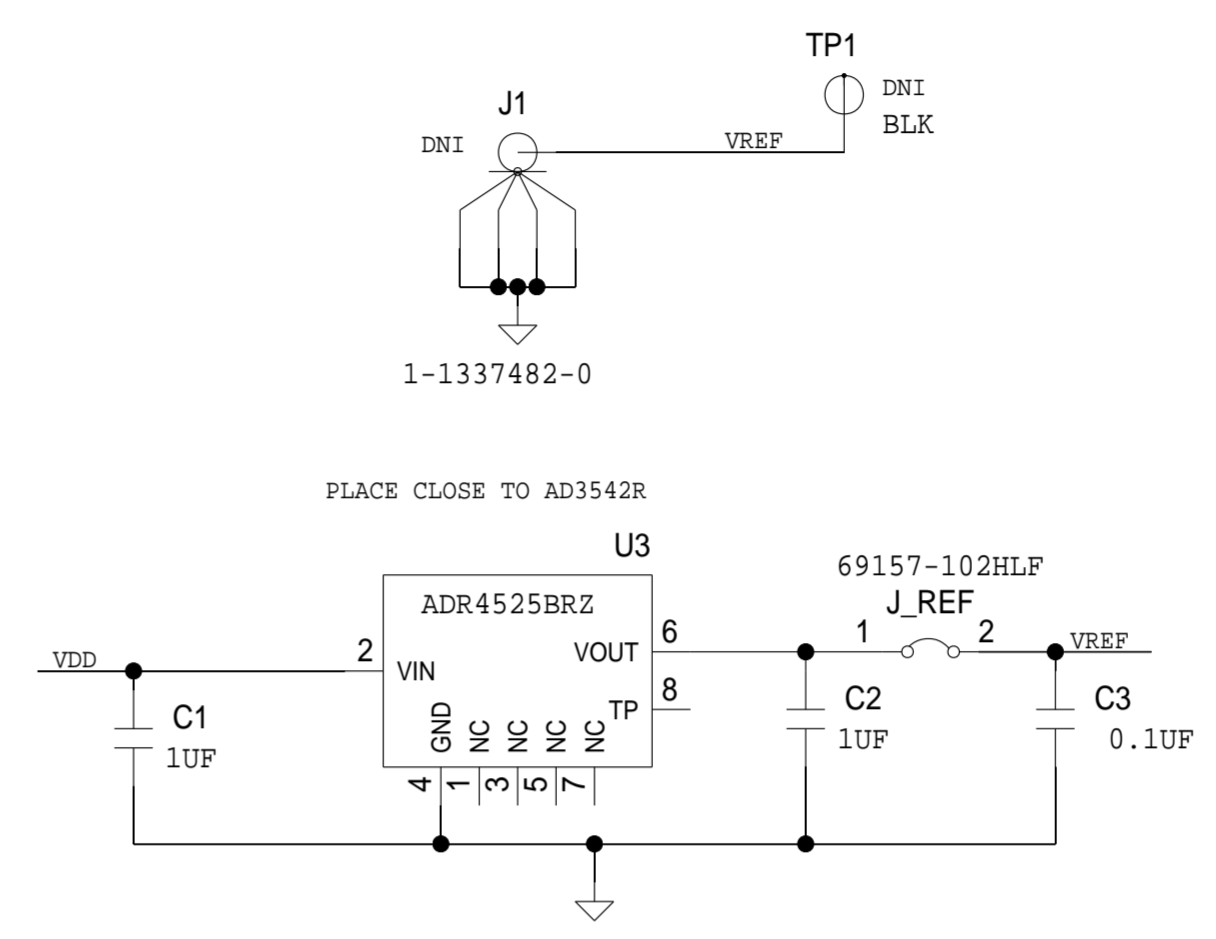
MISSING THE CLOCK, AND INTERRUPTION

	SCHEMATIC		
	HW TYPE : Customer Evaluation EVAL-AD3542RFMCZ		
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PTD ENGINEER ANTONIO JIMENEZ	SIZE D	SCALE 1:1	SHEET 2 OF 7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

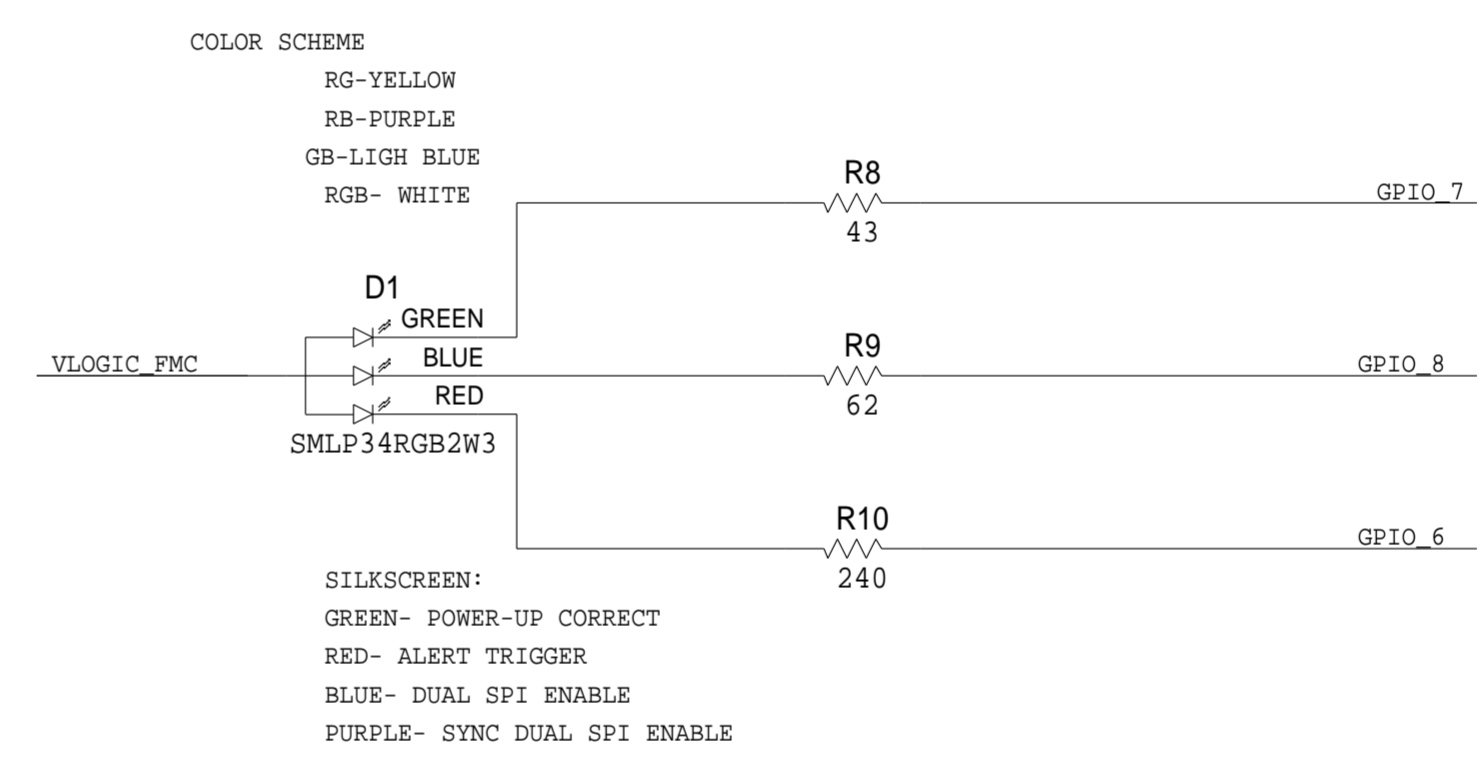
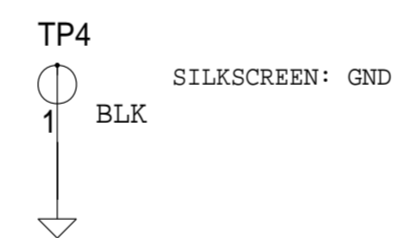
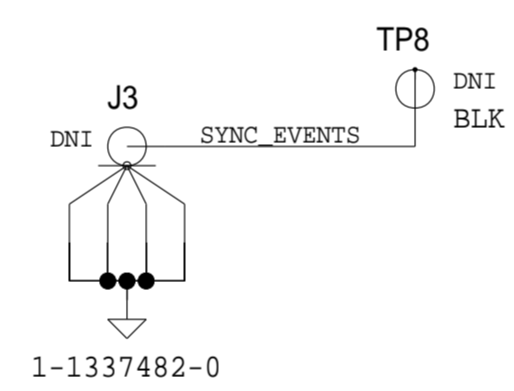
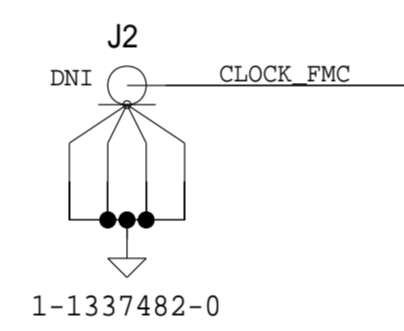
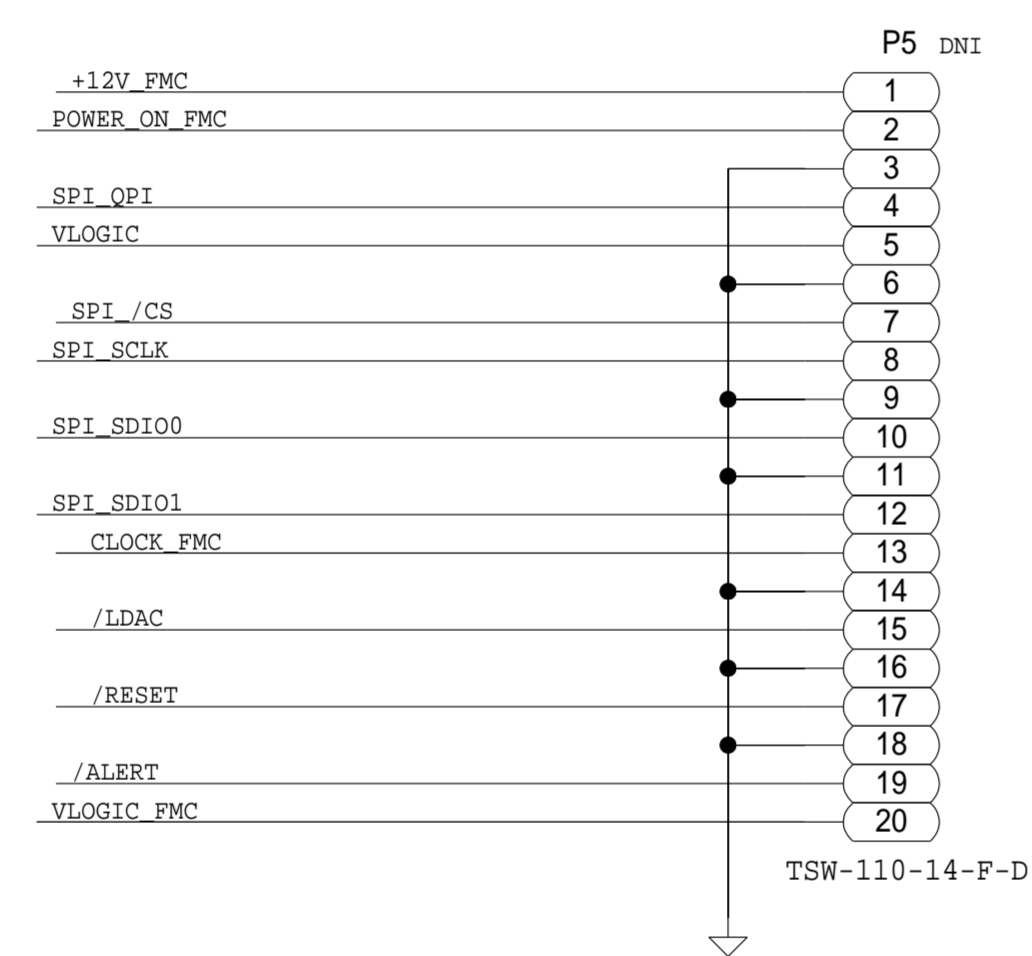


- SILKSCREEN:
 1- EXT PVDD
 2- EXT PVSS
 3- EXT VDD
 4- EXT DVDD
 5- EXT VLOGIC
 6- GND



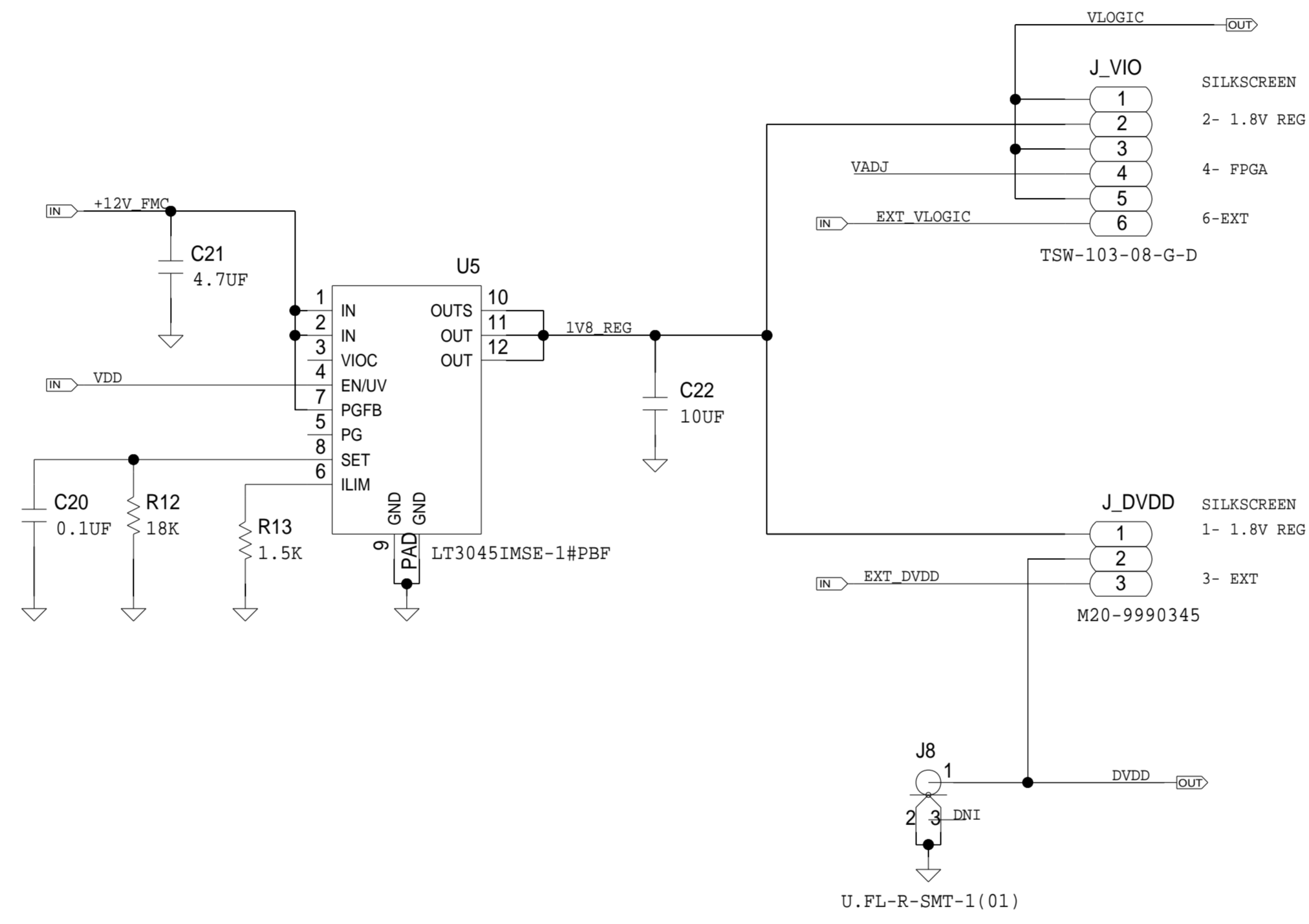
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	PTD ENGINEER ANTONIO JIMENEZ	SIZE D	SCALE 1:1
		SHEET 3 OF 7	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



	SCHEMATIC		
	HW TYPE : Customer Evaluation EVAL-AD3542RFMCZ		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-050892	REV D
	PTD ENGINEER ANTONIO JIMENEZ	SIZE D	SCALE 1:1
		SHEET 4 OF 7	

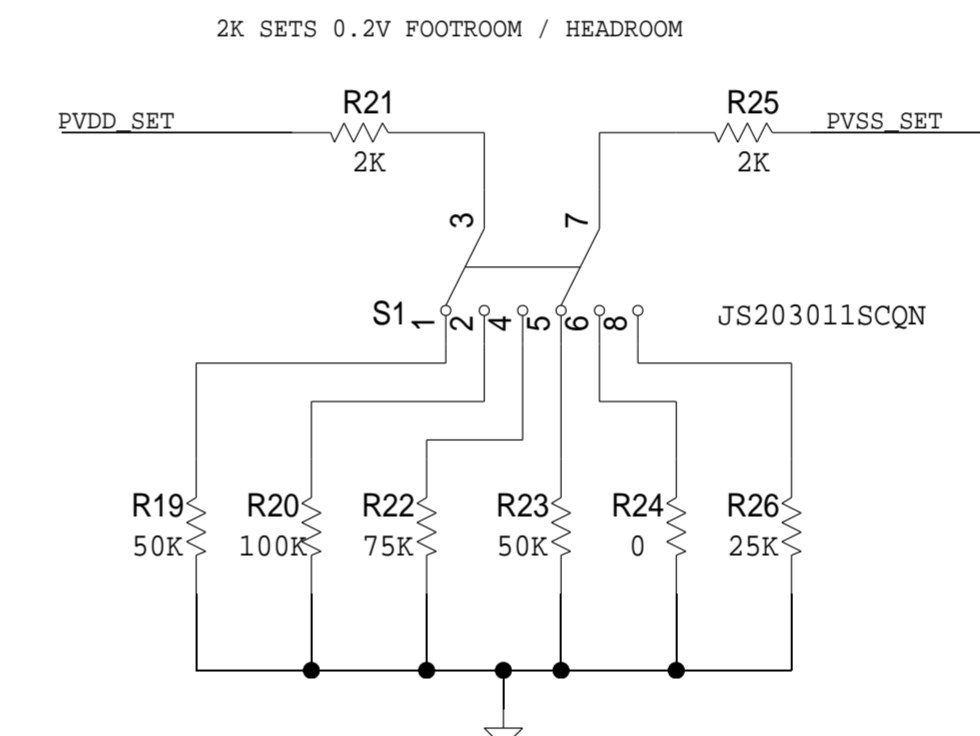
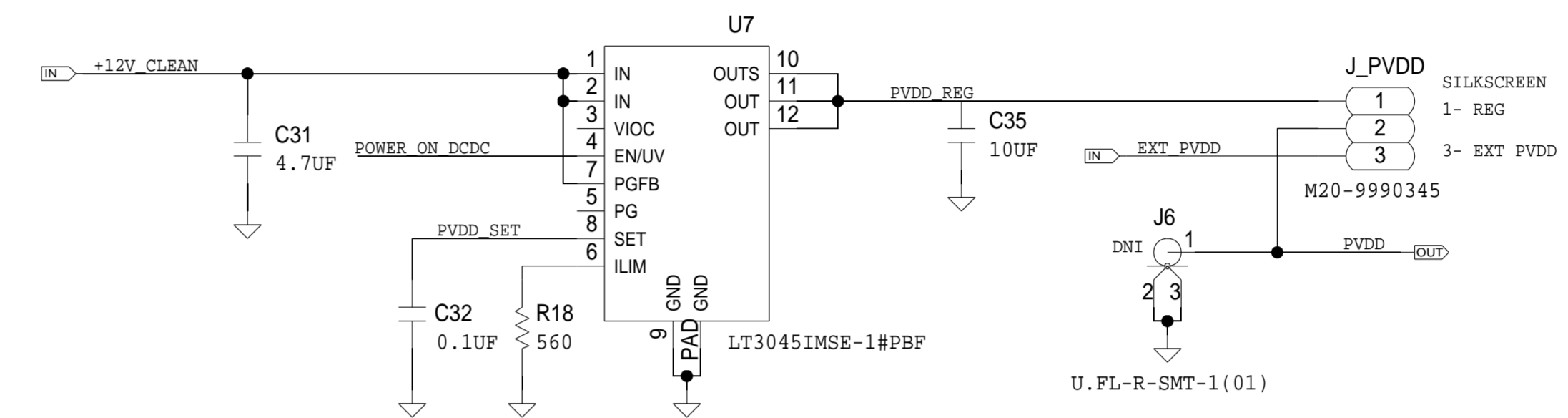
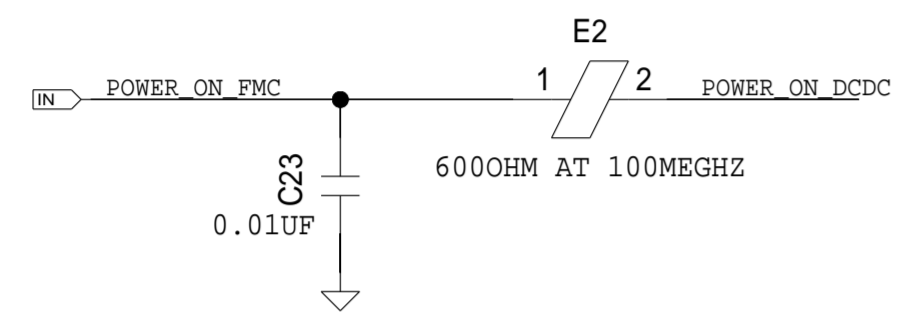
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REV	DESCRIPTION	DATE	APPROVED



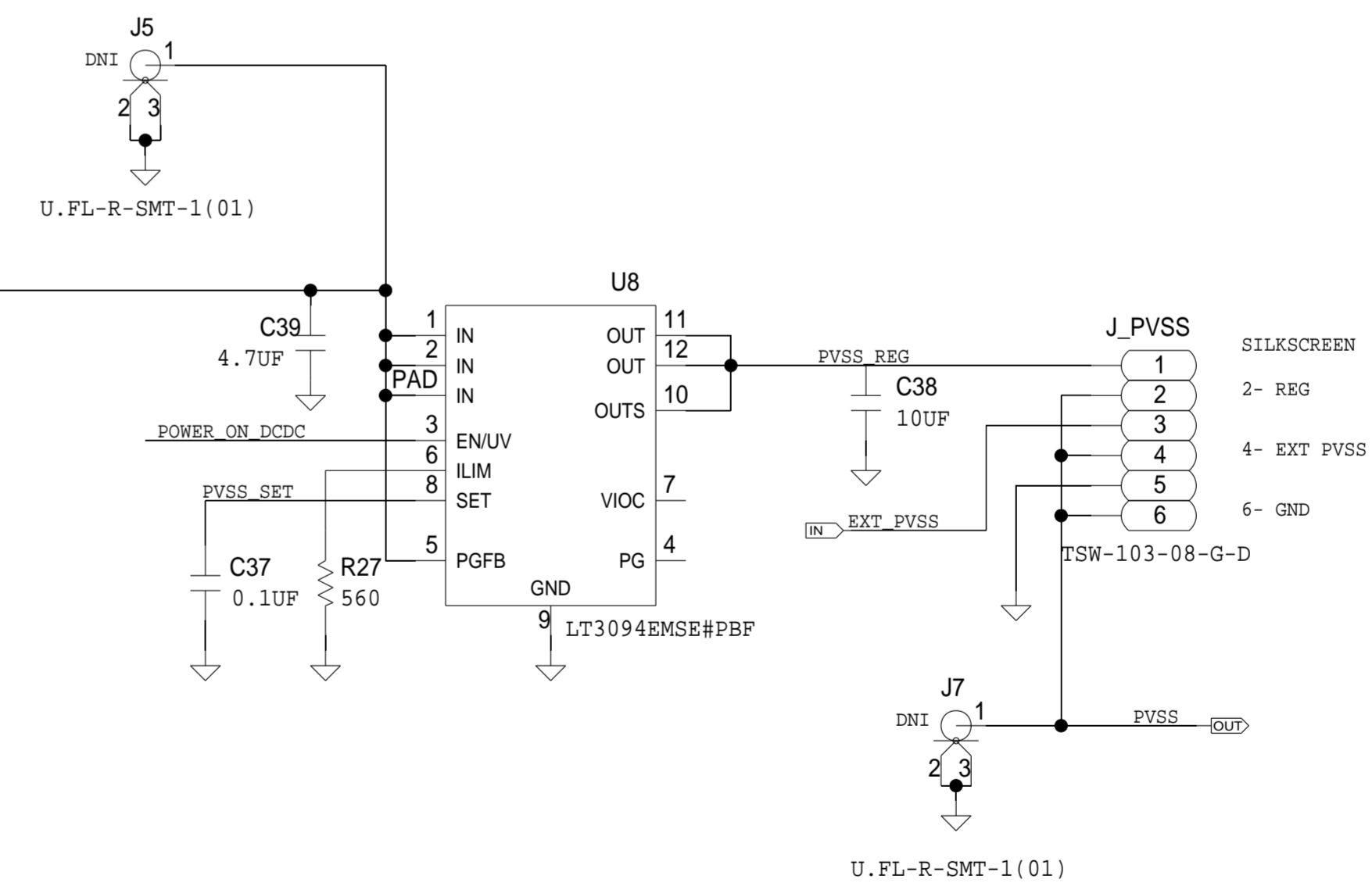
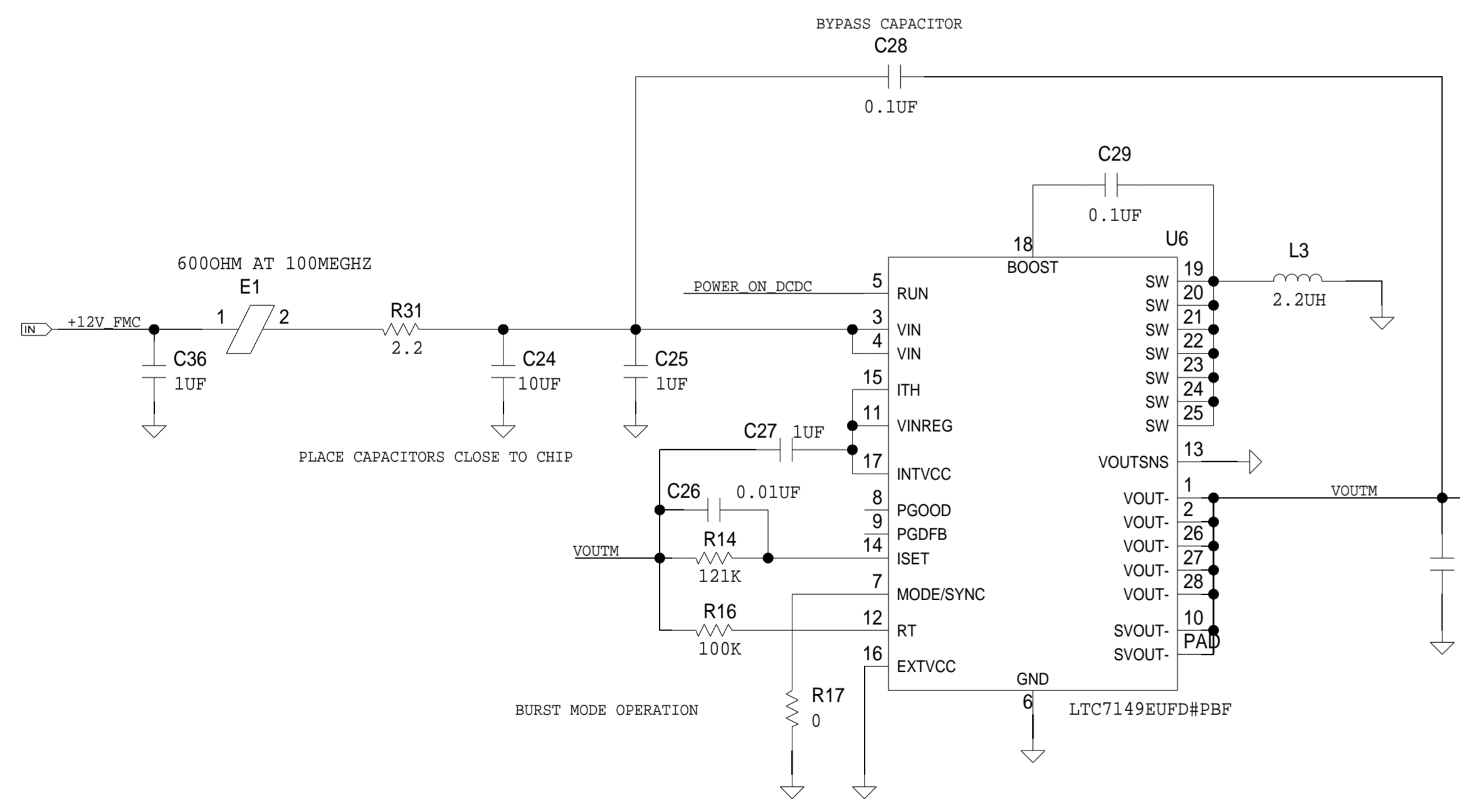
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PTD ENGINEER ANTONIO JIMENEZ	SIZE D	SCALE 1:1	SHEET 6 OF 7

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REV	DESCRIPTION	DATE	APPROVED



SILKSCREEN TEXT:
 +/-5V
 10V
 -2.5V TO 7V
 WARNING SIGN:
 DO NOT CHANGE VOLTAGE WITH BOARD POWERED ON.



	SCHEMATIC		
	HW TYPE : Customer Evaluation EVAL-AD3542RFMCZ		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-050892	REV D
	PTD ENGINEER ANTONIO JIMENEZ	SIZE D	SCALE 1:1

SHEET 7 OF 7