

AD9213-DUAL-EBZ Manual Calibration and Interleaving Guide

SCOPE

This Manual Calibration and Interleaving Guide provides detailed information on the recommended gain and timing calibration and an interleaving procedure using the example scripts provided. This document is intended to be used in conjunction with the Dual AD9213 Quick Start Guide.

CALIBRATION

Following is the high-level flow for manual matching calibration of the two AD9213 ADCs on the AD9213-DUAL-EBZ. For the manual calibration process, run the board in *SYNCHRONIZED 10G MODE*, which allows you to look at each AD9213 output separately (see the QuickStart Guide for setup instructions).

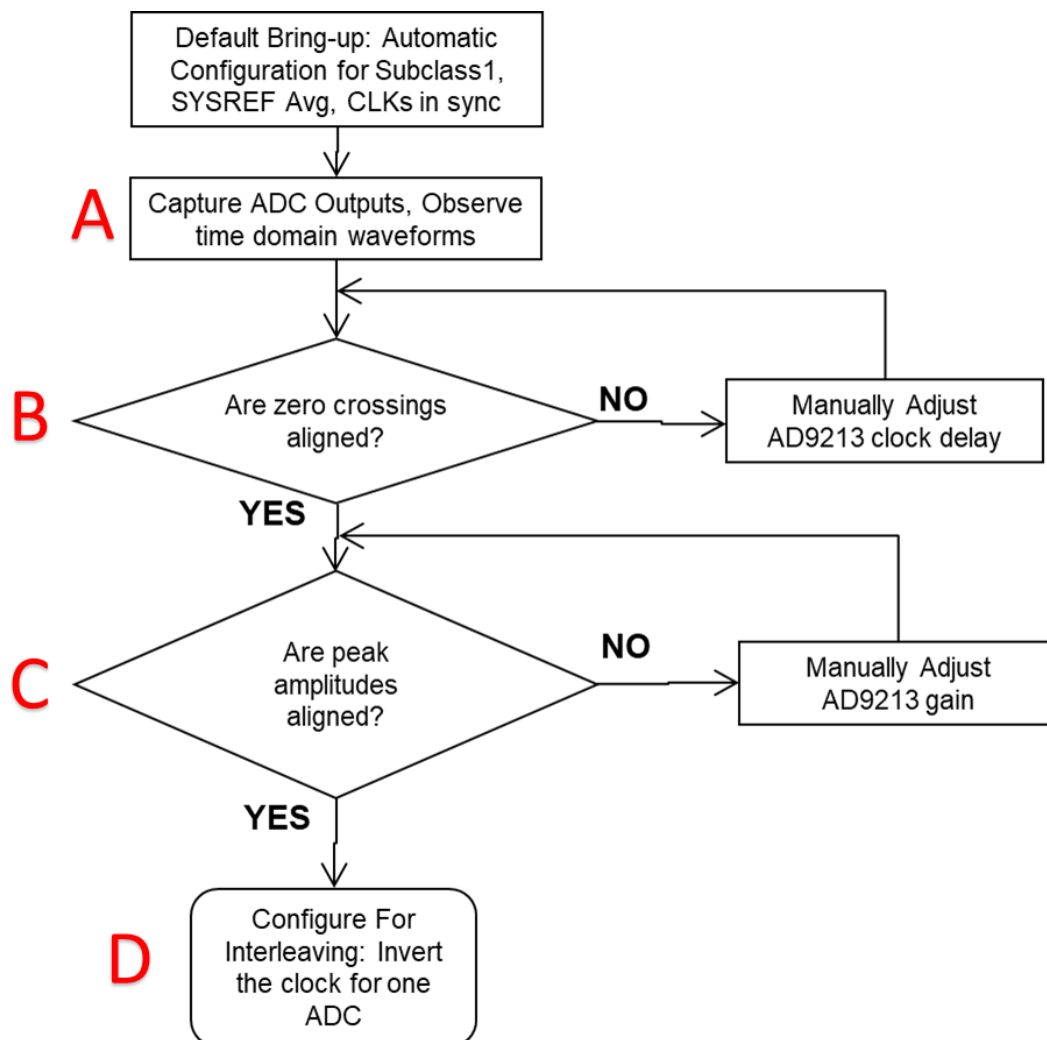


Figure 1 Manual Matching Calibration Flow

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STEP A Waveform Observation in IIO Oscilloscope

Follow the Dual AD9213 Quick Start Guide to bring up the AD9213-DUAL-EBZ and Stratix 10 in *SYNCHRONIZED 10G MODE*. Once the capture is set up in IIOScope apply a low frequency (3MHz – 200MHz) single-tone test signal to each of the AD9213s via a power splitter and phase-matched coax.

Coarsely aligned waveforms should be visible in the IIO Oscilloscope time domain waveform viewer.

STEP B Manual Time Alignment

Open an SSH connection to the board (using the steps described in the Dual AD9213 Quick Start Guide). Run the `Example_DualAD9213_Default_Settings.sh` script to set the entire system in default mode before attempting to apply calibration.

Apply a low frequency (3MHz – 200MHz) single-tone test signal. Capture the resultant time domain waveforms in IIO Oscilloscope. Use a small capture size (64 or 128). The waveforms will appear like the following:

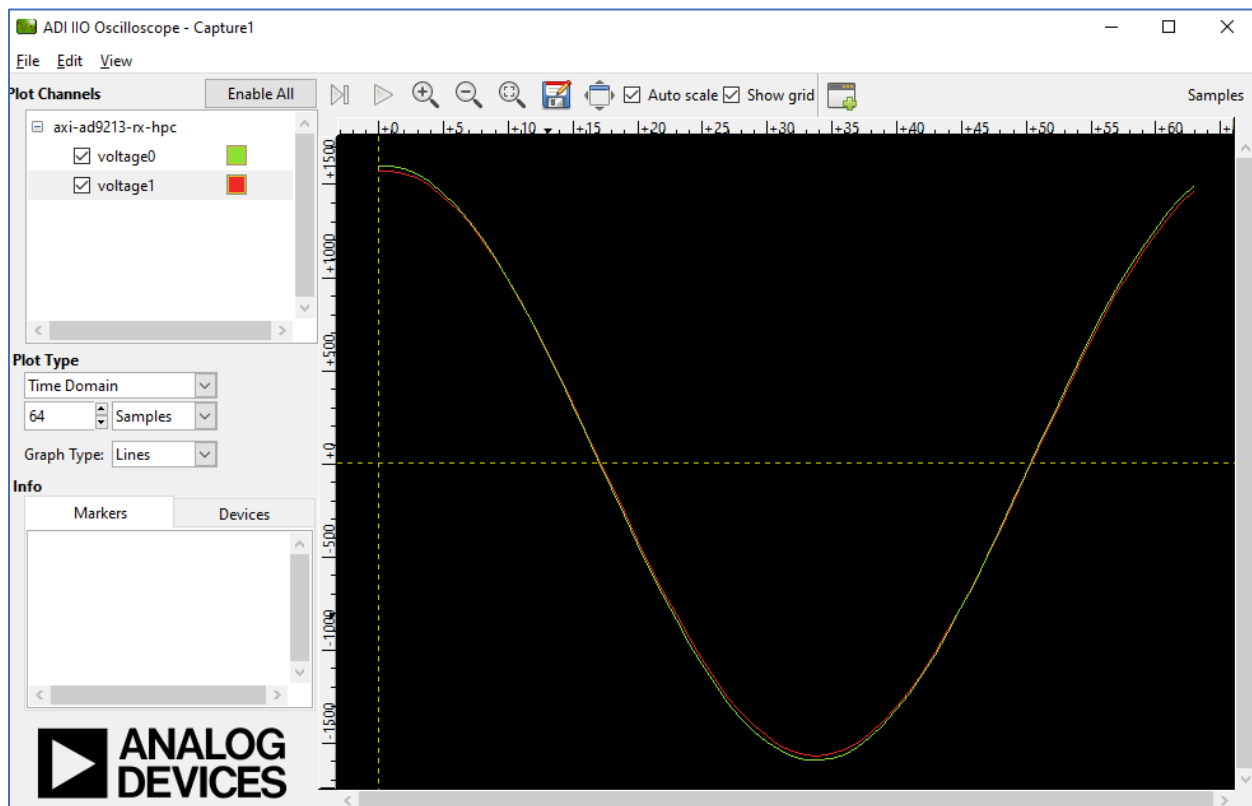


Figure 2 Example Pre-Calibration Waveforms in IIO Oscilloscope, $f_{IN} = 150.3\text{MHz}$, CaptureSize=64

The waveforms are aligned, with some mismatch visible.

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With the left mouse key, drag/draw a rectangle around one of the zero crossings, as shown below.

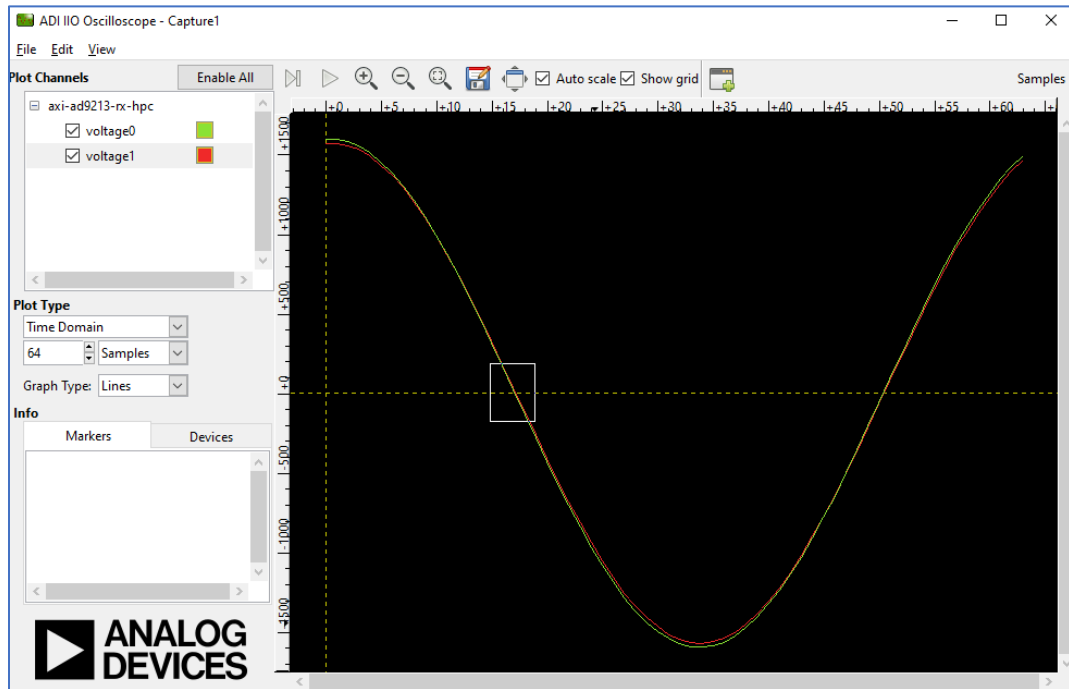


Figure 3 Left-click Drag/Draw a Rectangle Around a Zero-Crossing

Then left-click the mouse while the cursor is within the rectangle. The graph will zoom to the area within the rectangle.

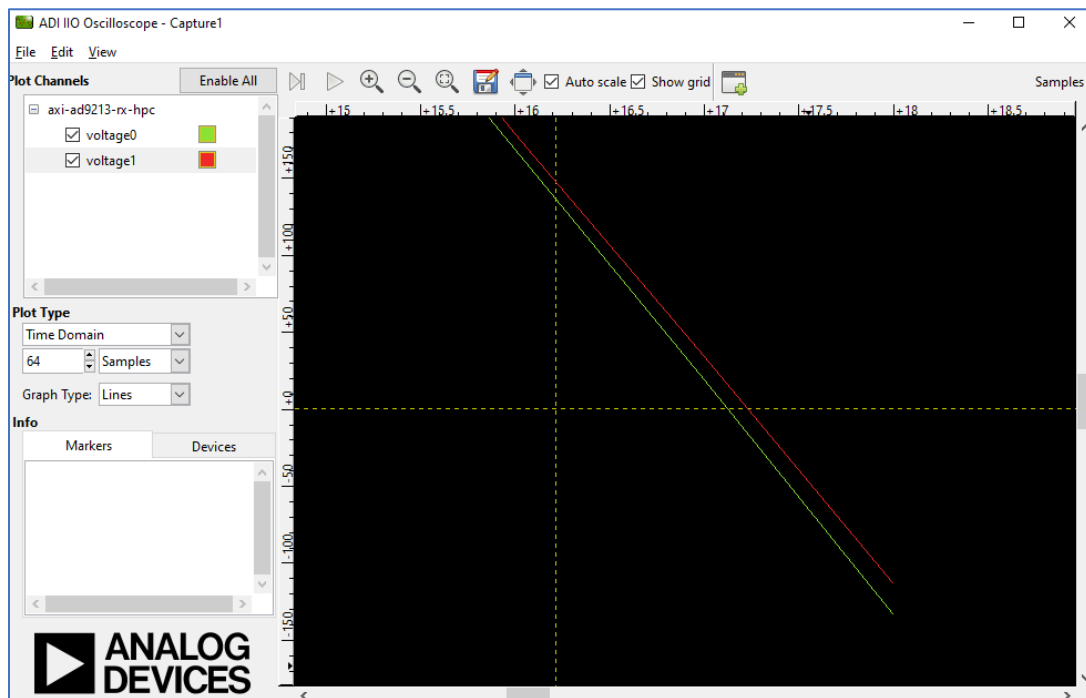


Figure 4 Example of Zoomed-In Zero Crossing

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A slight timing mismatch is observed and can be corrected by using the AD9213 clock delay registers.

SPI writes or reads to the AD9213 or the ADF4377 can be performed from the SSH console using the following function

```
lio_reg <device name _ index> <write address> <write data>  
lio_reg <device name _ index> <read address>
```

They can also be performed via the IIO Oscilloscope GUI (see the QuickStart Guide for details)

Modify the Example_DualAD9213_Timing_Alignment.sh script based on the following steps.

CLOCK DELAY REGISTER WRITE SEQUENCE

Writing AD9213 Register 0x150D = 0x02 enables half a fine-delay cell and a super-fine-delay cell

```
iio_reg ad9213_0 0x150D 0x02 #enable delay cells on AD9213_0  
iio_reg ad9213_1 0x150D 0x02 #enable delay cells on AD9213_1
```

This enables both AD9213s now have their clock delay cells enabled the same as each other.

Writing AD9213 Register 0x150E = 0x00 puts the default value into the clock delay registers.

```
iio_reg ad9213_0 0x150E 0x00 #set default clock delay for AD9213_0  
iio_reg ad9213_1 0x150E 0x00 #set default clock delay for AD9213_1
```

Choose one AD9213 to delay the clock on based on the relationship between the two waveforms in the capture. Write AD9213 Register 0x150E of one AD9213 to be a non-zero value.

```
iio_reg ad9213_0 0x150E 0x00 #set default clock delay for AD9213_0  
iio_reg ad9213_1 0x150E 0x30 #set non-default clock delay for AD9213_1
```

Run the modified script and observe how one waveform zero-crossing moves with respect to the other. Continue modifying the script and running it until the zero-crossings of each waveform align as close as possible.

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STEP C Manual Gain Adjustment

Again capture the waveforms in IIO Oscilloscope. Locate the sinusoidal peaks of the waveforms and draw (left-click and drag) a zoom rectangle around one of the peaks.

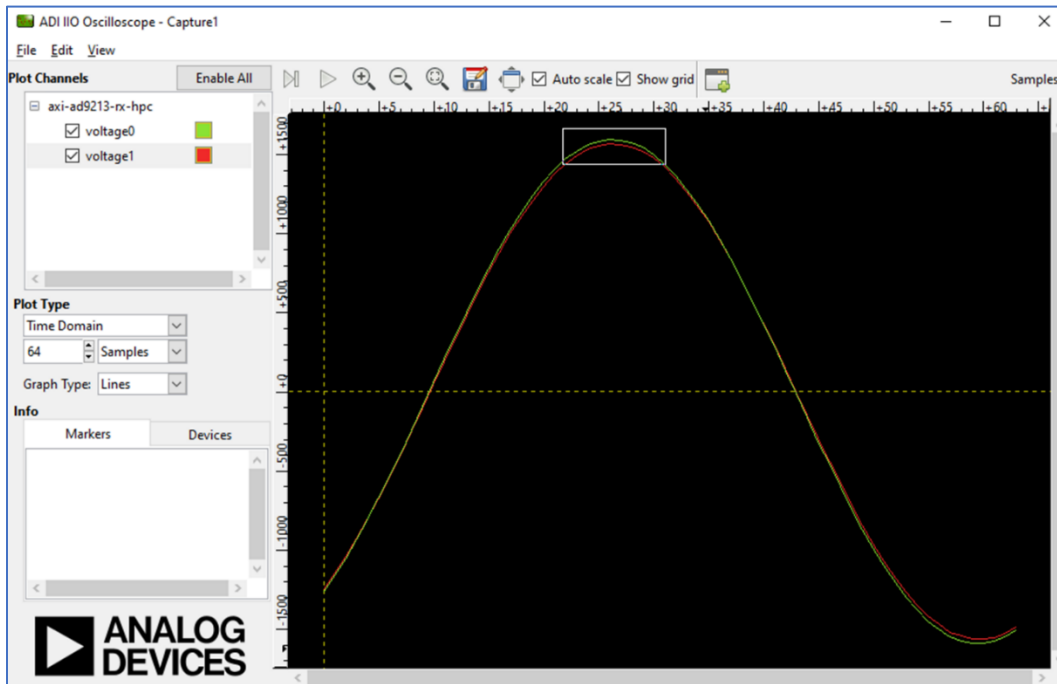


Figure 5 Left-click/drag a rectangle around the waveform peak area

Then left-click the mouse while the cursor is within the rectangle. The graph will zoom to the area within the rectangle.

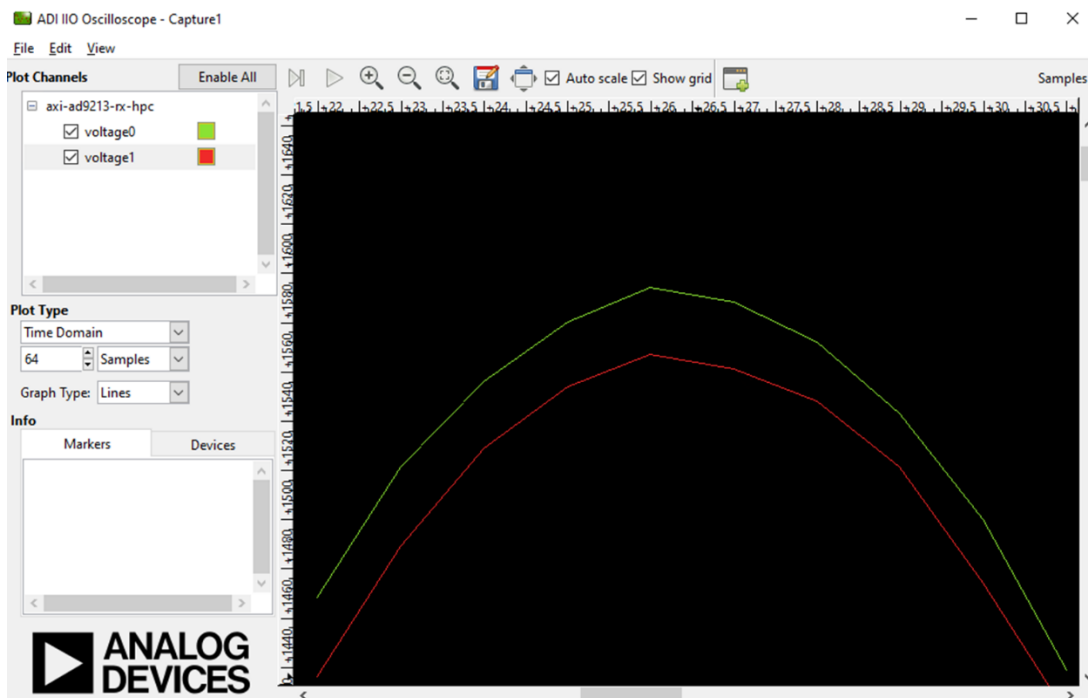


Figure 6 Example of Zoomed-in Waveform peak

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A slight amplitude mismatch is observed and can be corrected by using the AD9213 gain adjustment registers.

Modify the Example_DualAD9213_Gain_Alignment.sh script based on the following steps

GAIN ADJUSTMENT REGISTER WRITES

Writing AD9213 0x1612 and 0x1613 gain registers to default gain settings

```
iio_reg ad9213_0 0x1612 0x00
```

```
iio_reg ad9213_0 0x1613 0x40
```

```
iio_reg ad9213_1 0x1612 0x00
```

```
iio_reg ad9213_1 0x1613 0x40
```

Writing transfer bits to put the gain register settings into effect

```
iio_reg ad9213_0 0x1600 0x01 #transfer bit required to put 0x16xx writes into effect
```

```
iio_reg ad9213_1 0x1600 0x01 #transfer bit required to put 0x16xx writes into effect
```

Choose one AD9213 to adjust the gain on. Write AD9213 Register 0x1612 (LSBs) and/or Register 0x1613 (MSBs) of one AD9213 to be a non-default value.

```
iio_reg ad9213_0 0x1612 0x00 #default
```

```
iio_reg ad9213_0 0x1613 0x40 #default
```

```
iio_reg ad9213_1 0x1612 0x80 # set non-default value written to AD9213_1
```

```
iio_reg ad9213_1 0x1613 0x40 #default
```

```
iio_reg ad9213_0 0x1600 0x01 #transfer bit required to put 0x16xx writes into effect
```

```
iio_reg ad9213_1 0x1600 0x01 #transfer bit required to put 0x16xx writes into effect
```

Run the modified script and observe how the waveform peak amplitudes move with respect to each other. Continue modifying the script and running it until the peak amplitudes of each waveform align as close as possible.

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After this is accomplished, both timing and gain have been matched. The waveforms in IIO Oscilloscope will now be closely aligned (visually), as shown in the example below.

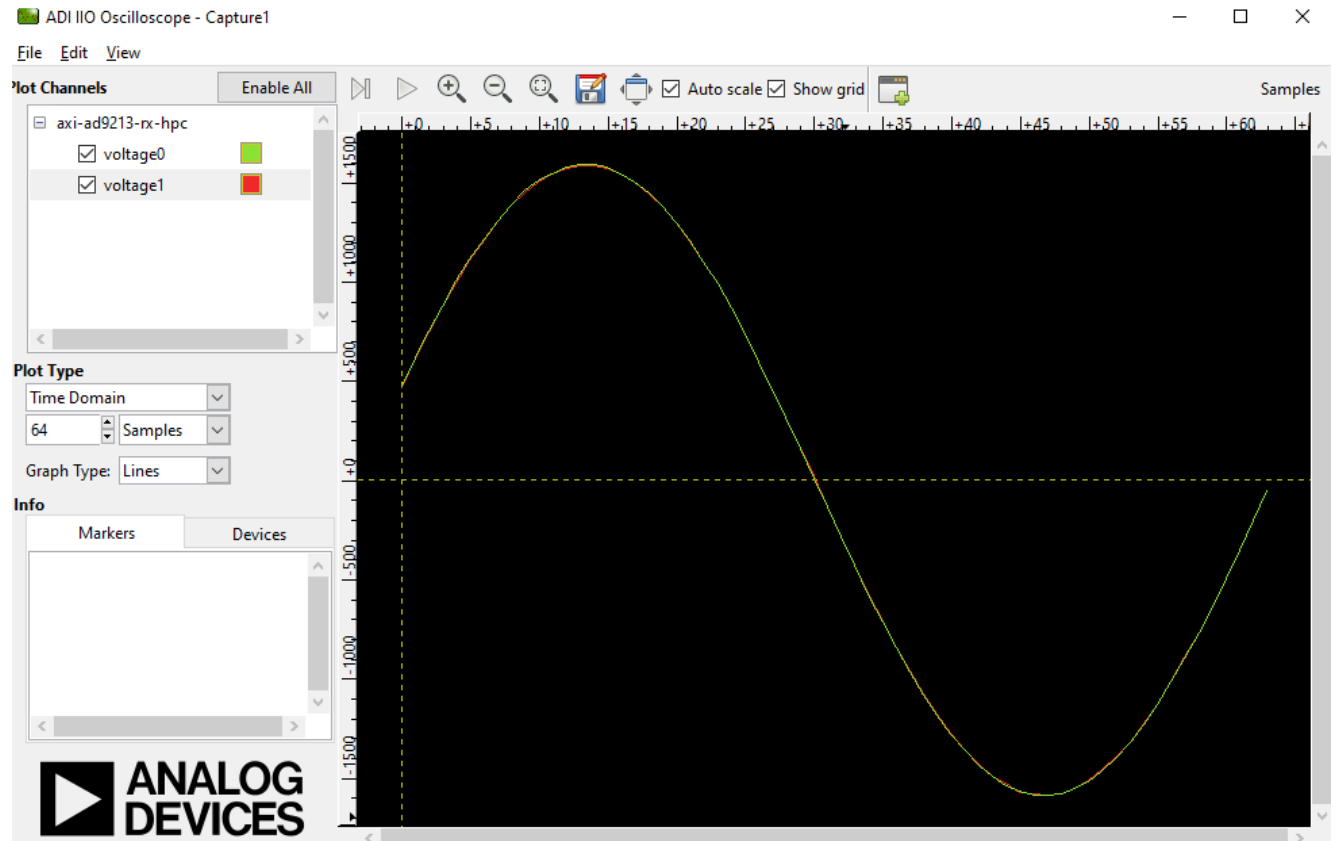


Figure 7 Waveforms After Manual Calibration

At this point, the manual calibration process is complete. Save off the modified scripts with the values obtained. These will be used in the interleaved operation below.

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STEP D Configure for Interleaving; Invert the Clock for One ADC

Follow the Dual AD9213 Quick Start Guide to bring up the AD9213-DUAL-EBZ and Stratix 10 in *INTERLEAVED 20G MODE*. Once the capture is set up in VisualAnalog, apply the same analog input signal to the two AD9213s via a power splitter and phase-matched coaxes.

Open an SSH connection to the board (Steps described in the Dual AD9213 Quick Start Guide)

Run scripts in the following order

1. Example_DualAD9213_Default_Settings.sh
2. Example_DualAD9213_Timing_Alignment.sh
3. Example_DualAD9213_Gain_Alignment.sh

The ADF4377 provides the 10GHz sampling clock to both AD9213s. The clocks to either of the two AD9213s can be inverted by writing Register 0x17 = 1 on the ADF4377 whose clock is to be inverted.

The following code sequence includes SPI writes to the AD9213 which configure the AD9213 to accept a sample clock frequency change. Even though the sample clock frequency is not changing in this case, the inversion of the clock involves a momentary change in the clock. The AD9213 is better equipped to accept the clock inversion when the clock frequency change procedure is followed. See the AD9213 datasheet CHANGING SAMPLE CLOCK FREQUENCY WITHOUT POWER DOWN section for more information

Run the Example_DualAD9213_Robust_Invert Script to set up the clocking for Interleaving

Write AD9213_1 Register 0x332 = 0x02 to alert AD9213 that the user is changing the clock.

```
iio_reg ad9213_1 0x0332 0x02
```

Read Register 0x1614, Bit 0. Wait for this bit to go high, which indicates that the user can change the encode clock rate or clock

```
iio_reg ad9213_1 0x1614
```

Write Register 0x1602 = 0x01. This selects the coefficient location for Clock Rate 1 (the next/new clock rate, default is Clock Rate 0).

```
iio_reg ad9213_1 0x1602 0x01
```

Invert the clock being created by ADF4377_1

```
iio_reg adf4377_1 0x17 0x80 #
```

Write Register 0x1614, Bit 1 = 1. This notifies the AD9213 that the sample clock frequency has been changed

```
iio_reg ad9213_1 0x1614 0x03
```

Read Register 0x1614, Bit 2. Wait for this bit to go high which indicates that the change is complete

```
iio_reg ad9213_1 0x1614
```


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NOTE: Running the interleaving scripts could lead to the FPGA links being brought down. In case that happens reset the FPGA links using the `Example_Reset_FPGA_Links.sh`

Capture and view the waveforms in VisualAnalog. An interleaving spur will be present at (10GHz - input frequency). The spur height will depend on how well the manual gain and timing alignment was performed. With Manual Calibration good alignment at high analog input frequencies is challenging. Additional manual gain and timing calibration can be performed using the interleaving spur height as a guide.

NOTE: For additional guidance on automated calibration, please reach out to your ADI contact